

PG132-A02

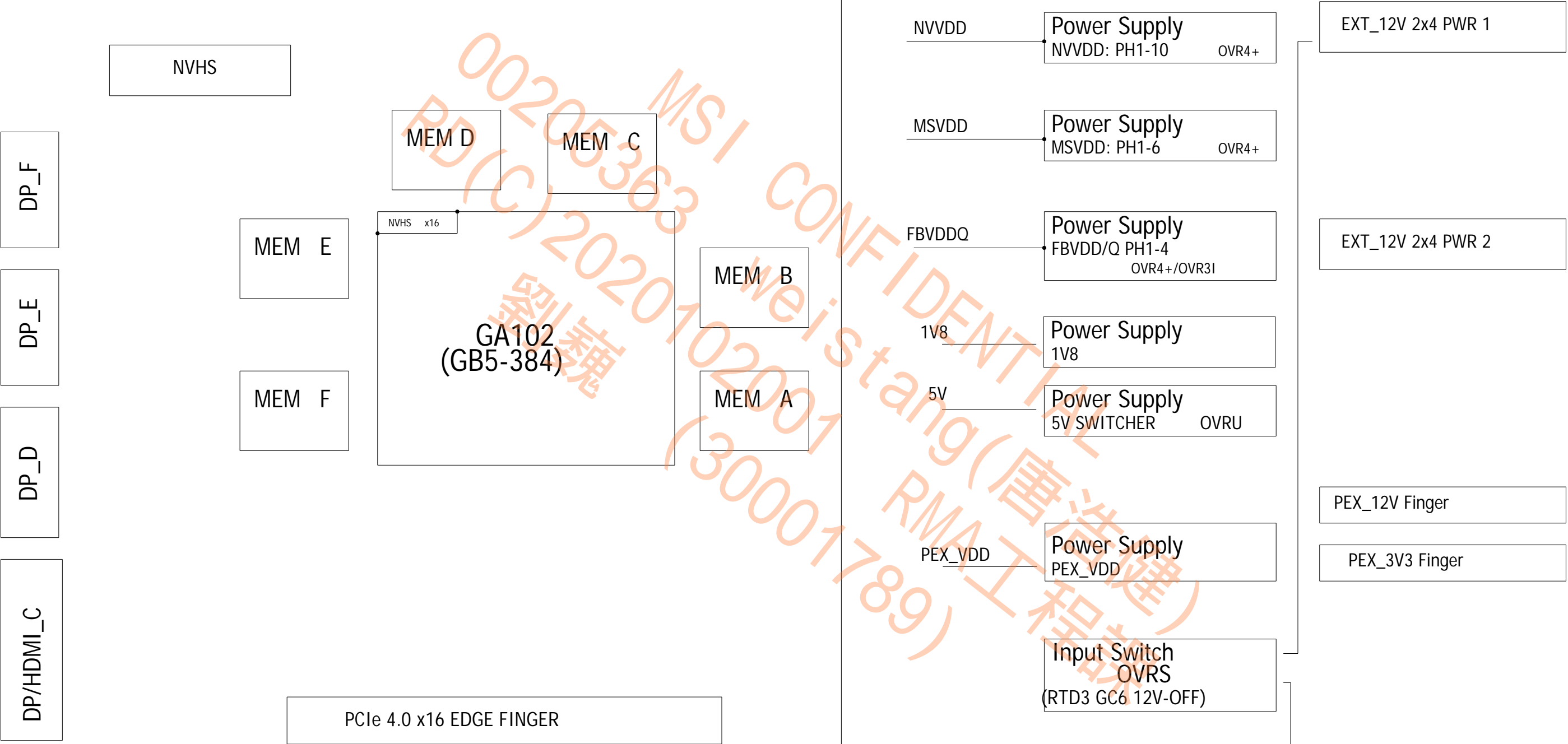
320W, FH Std PCB, 320b, GDDR6X 2CH x16  
DP + DP + DP + HDMI

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Block Diagram

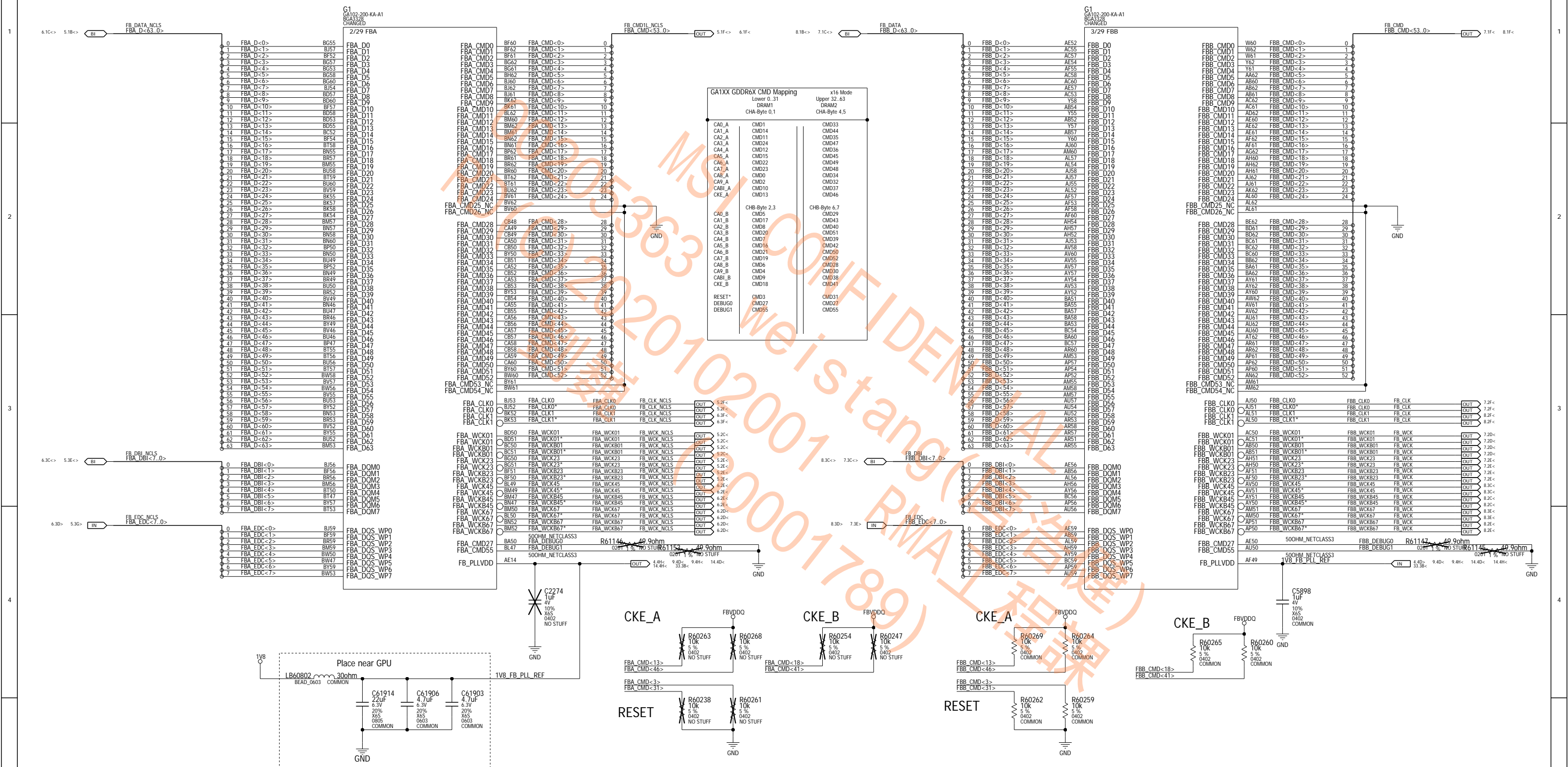


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MEMORY: GPU Partition A/B



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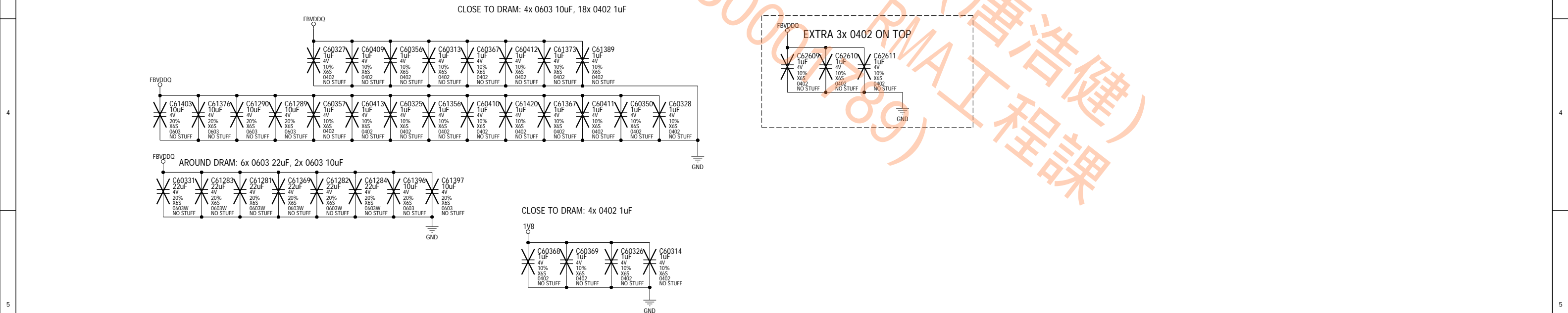
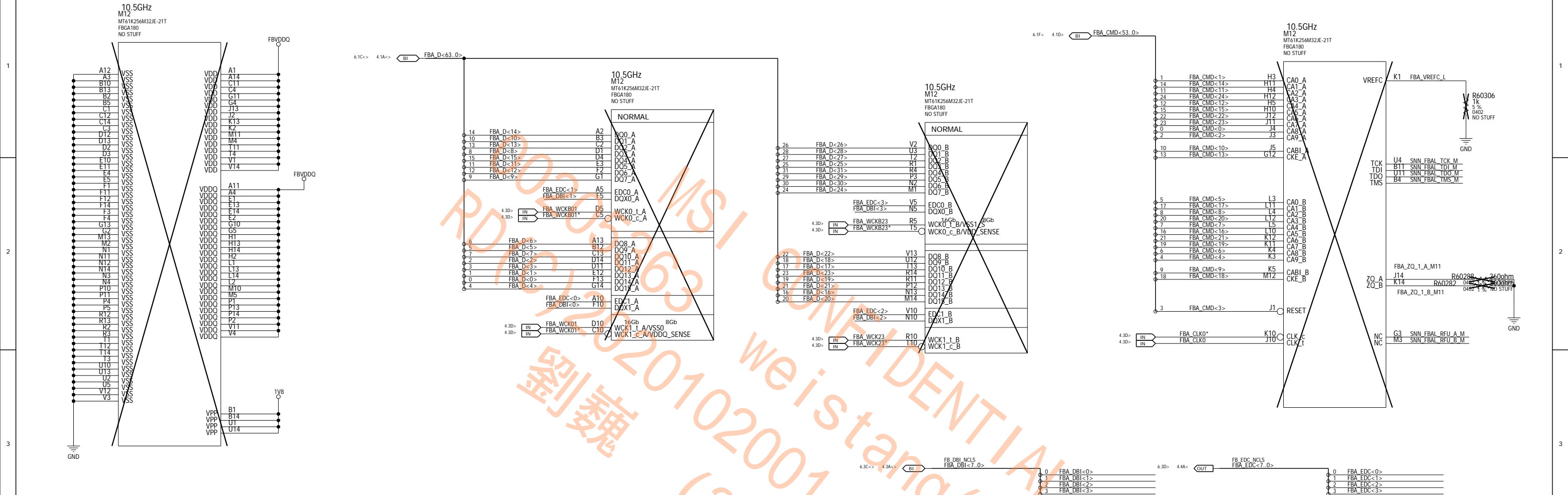
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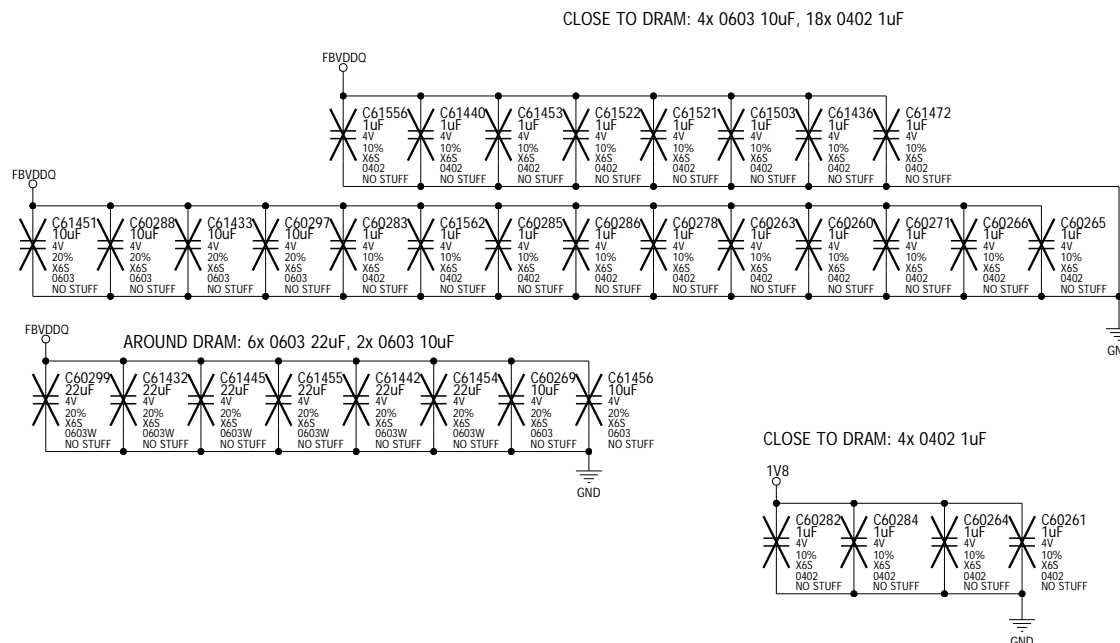
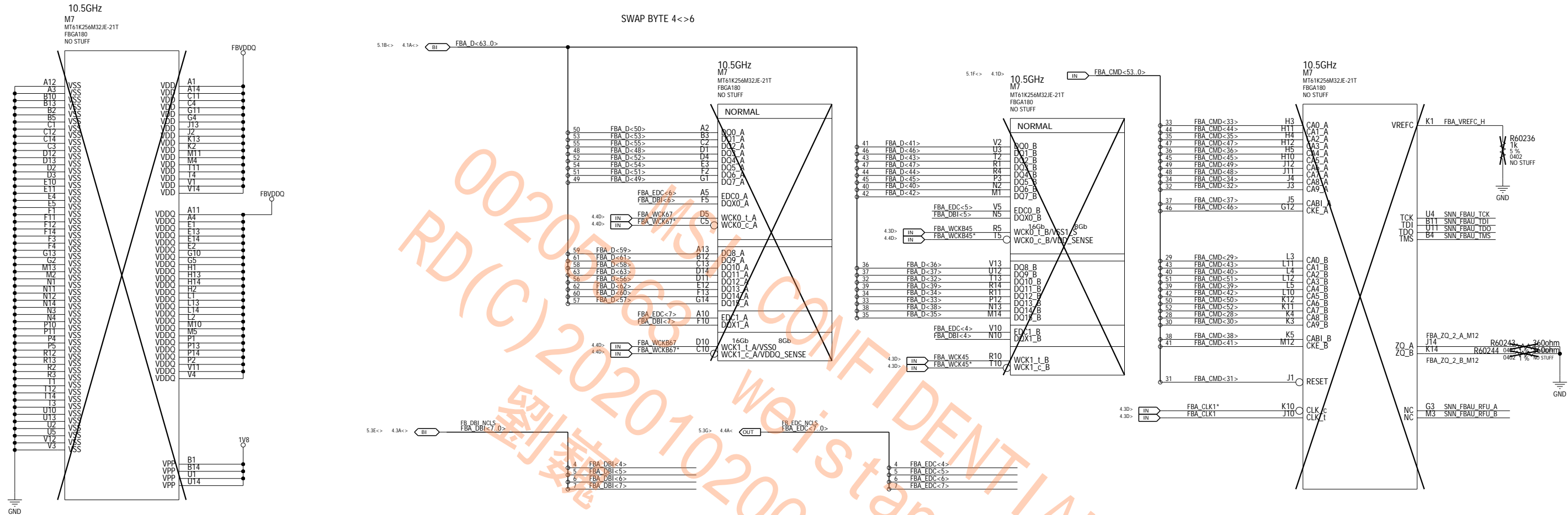
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PAGE DETAIL	MEMORY: GPU PARTITION A/B

MEMORY: FBA Partition 31..0



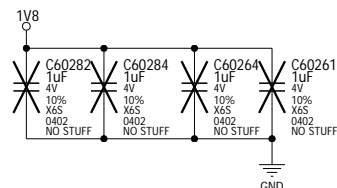
MEMORY: FBA Partition 63..32



EXTRA 1x 0402 ON BOT



CLOSE TO DRAM: 4x 0402 1uF



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PAGE DETAIL	MEMORY: FBA PARTITION[63:32]

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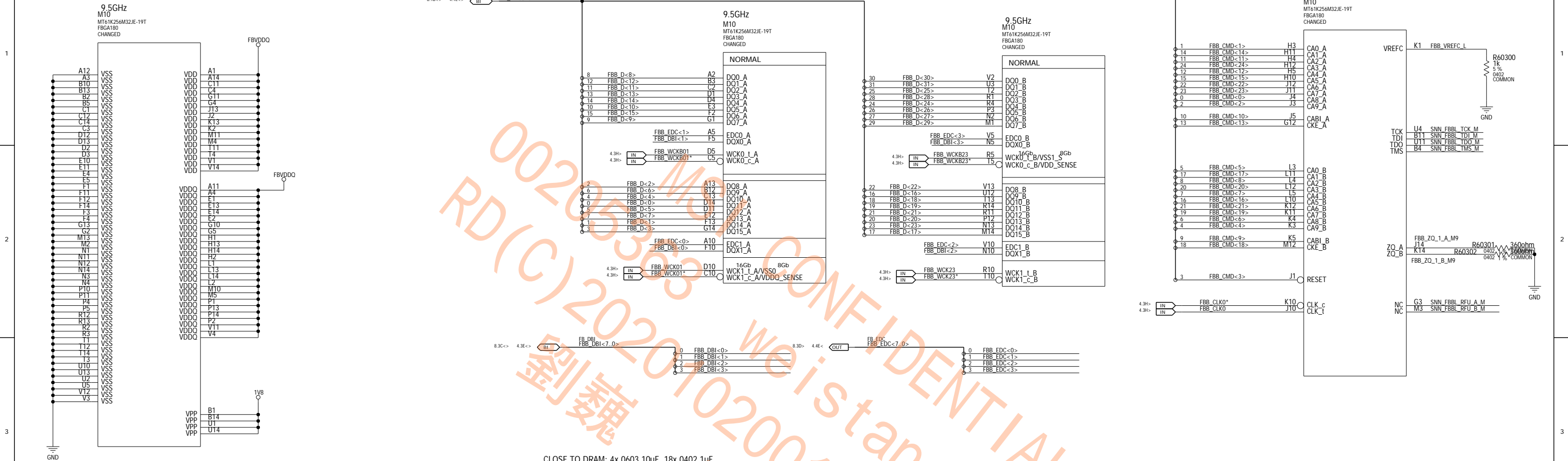
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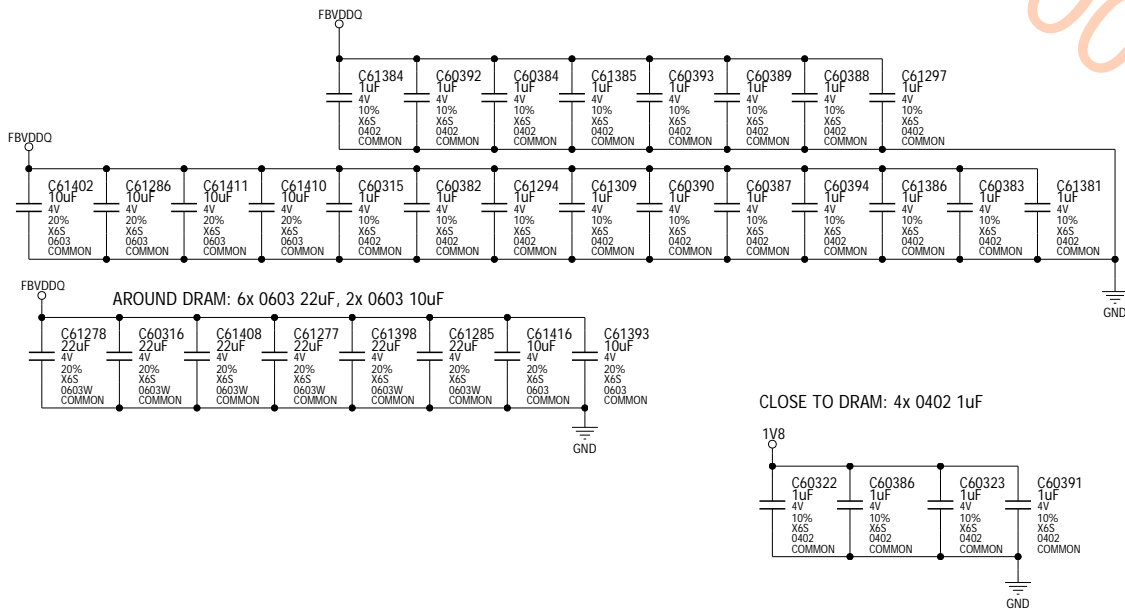




MEMORY: FBB Partition 31..0



CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



CLOSE TO DRAM: 4x 0402 1uF

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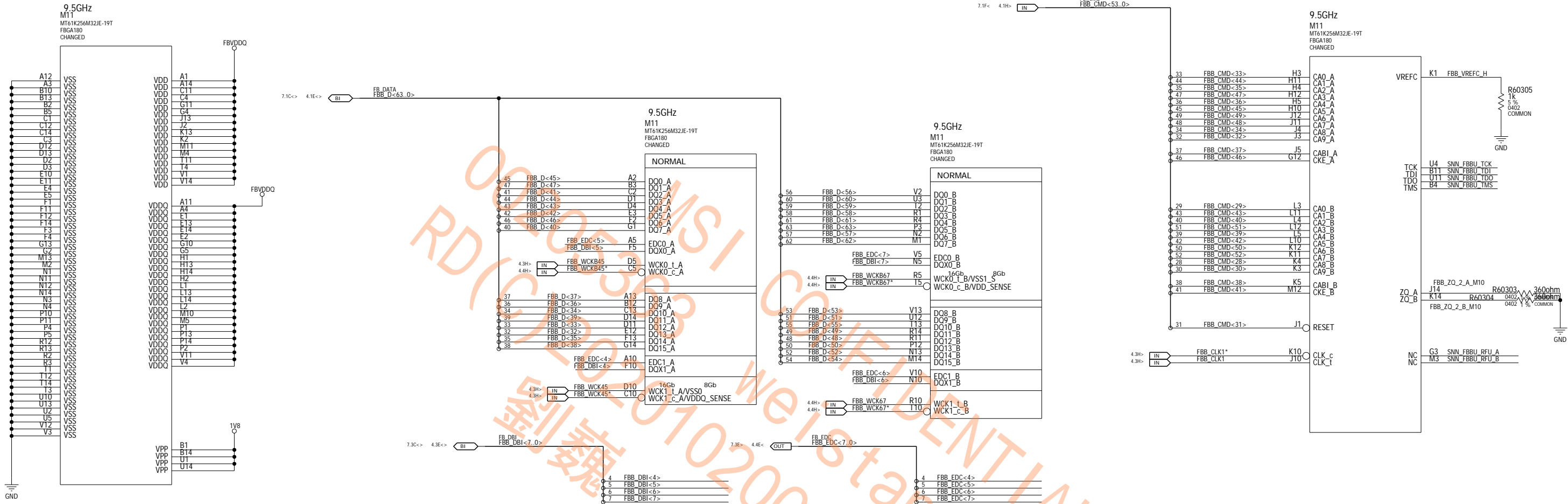
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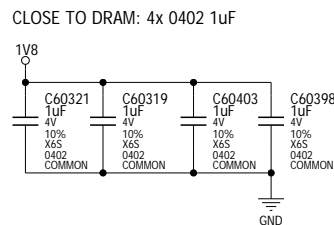
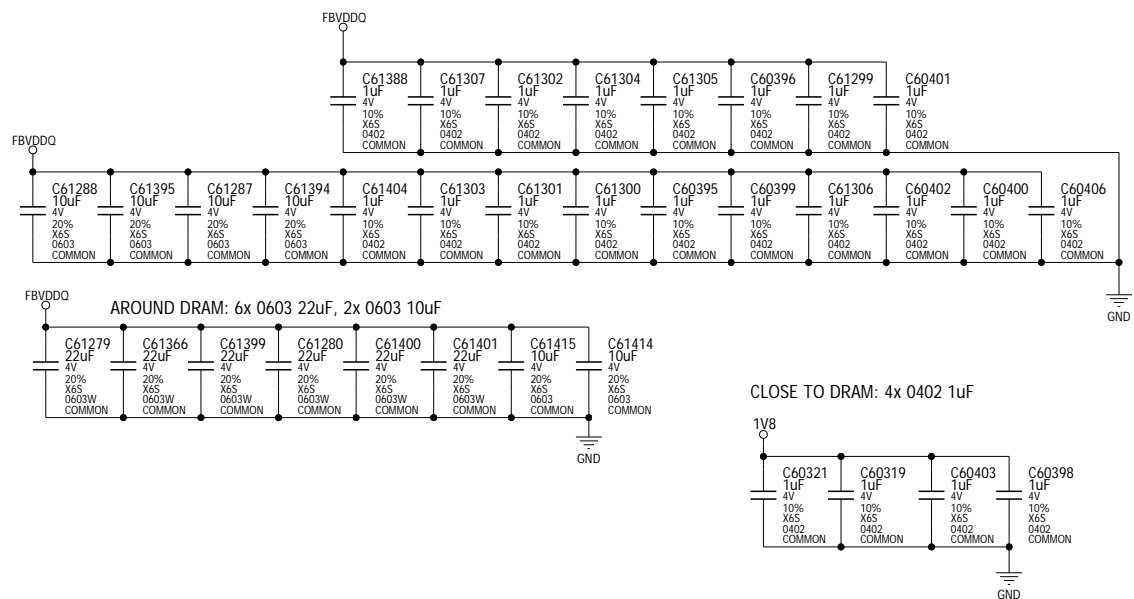
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MEMORY: FBB Partition 63..32

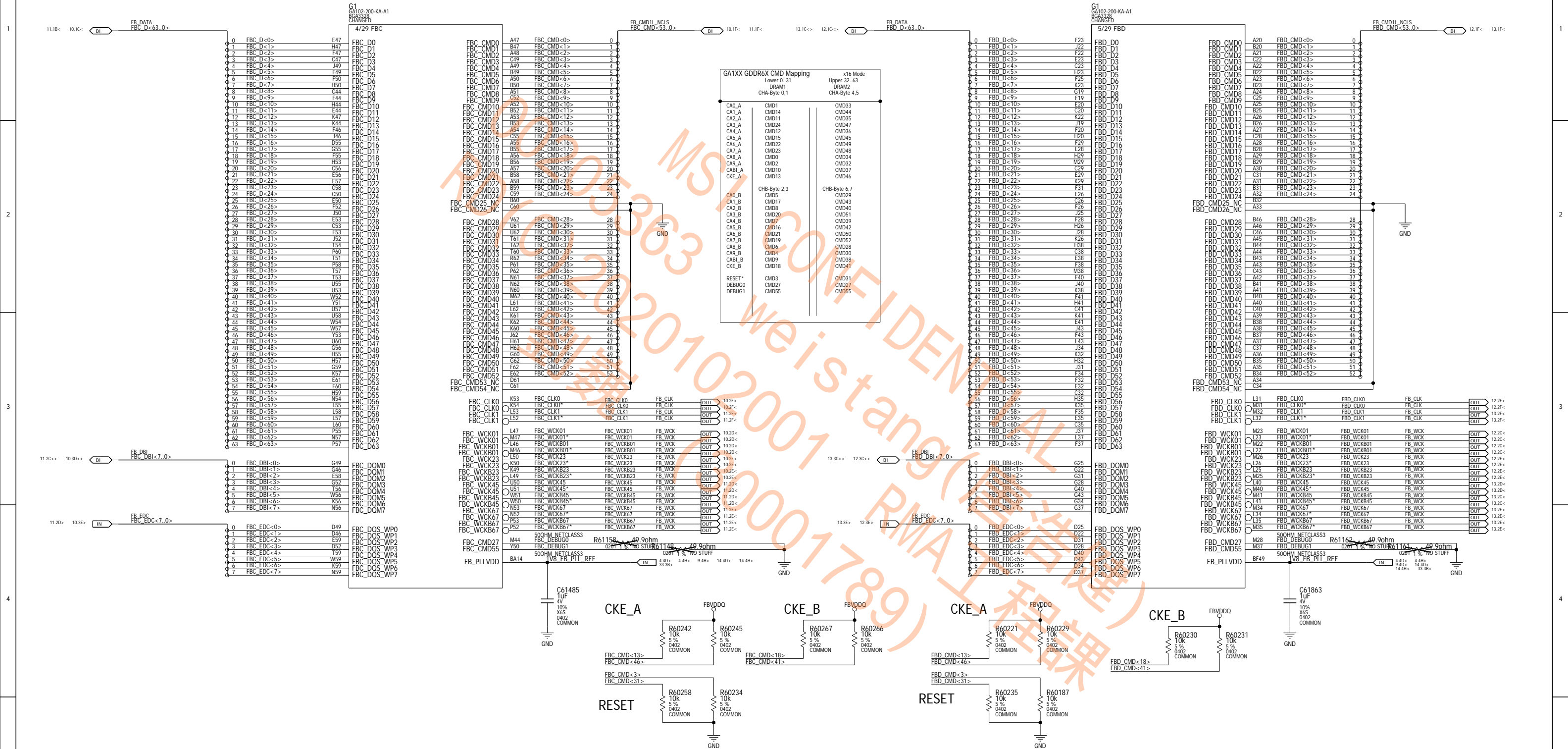


CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF





MEMORY: GPU Partition C/D



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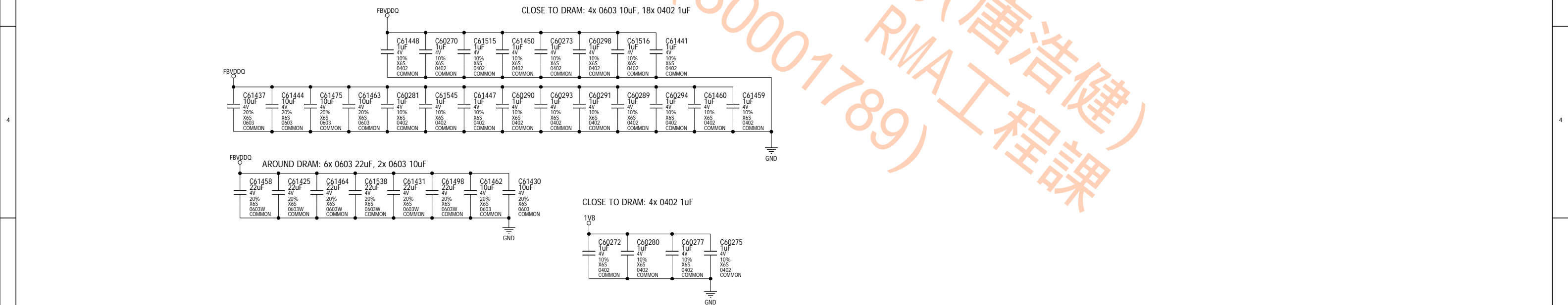
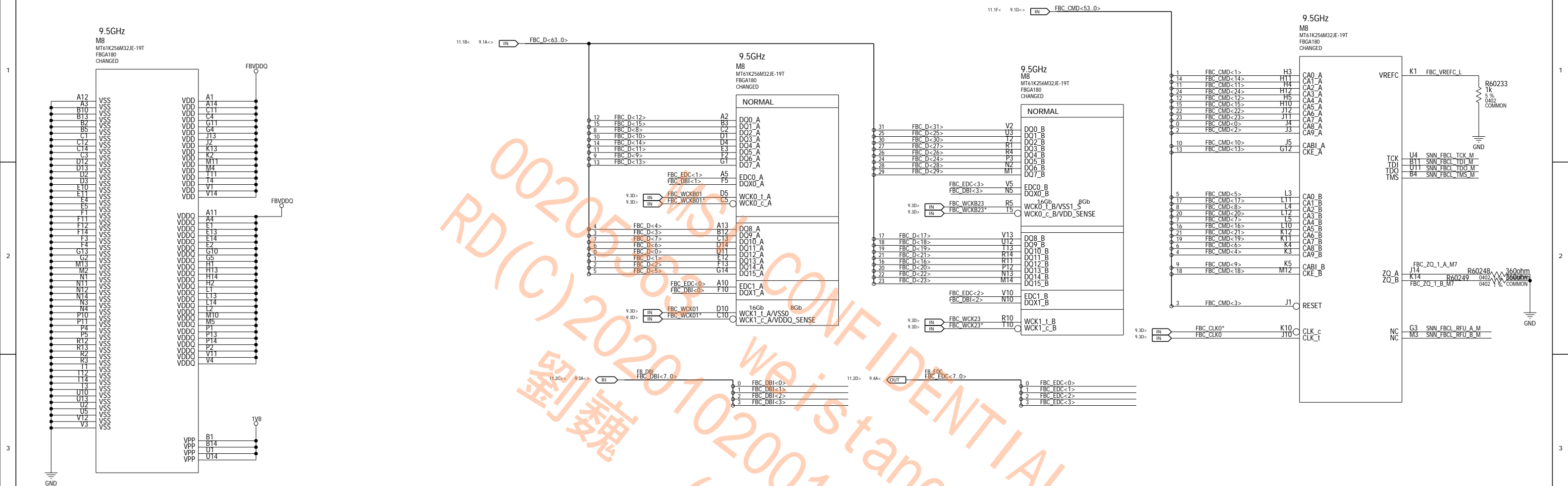
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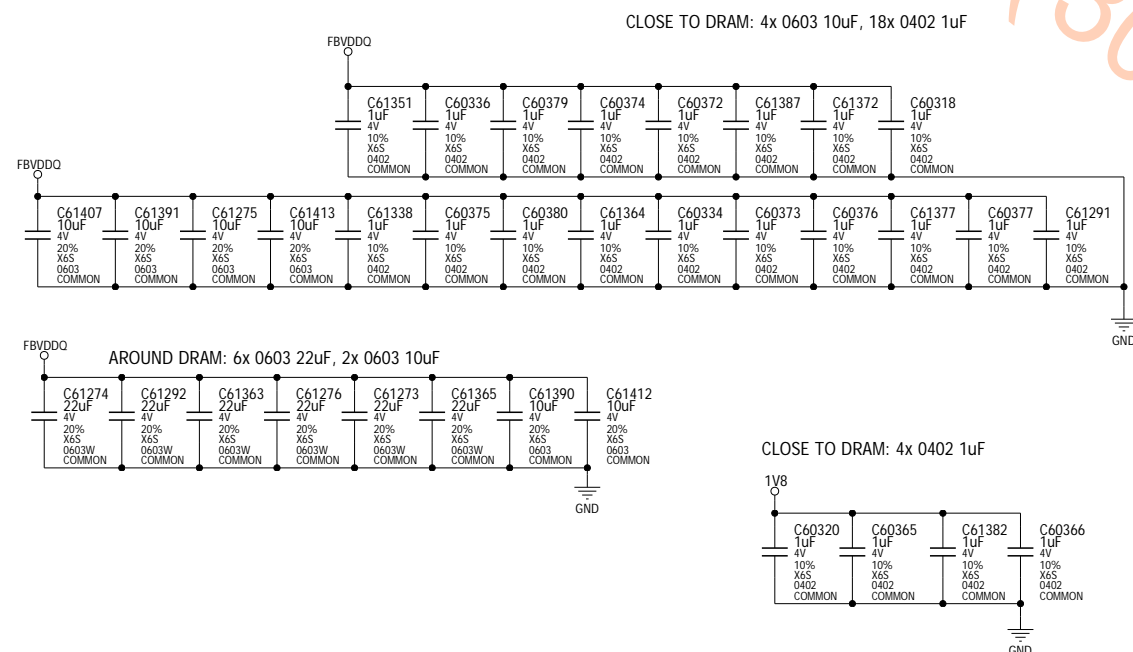
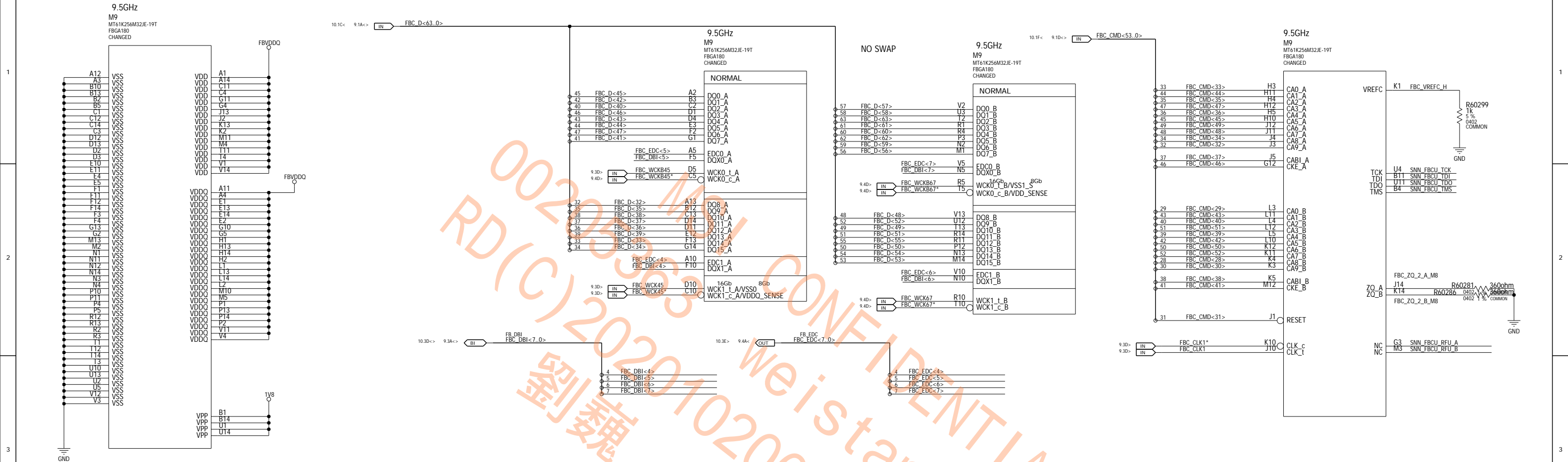
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MEMORY: FBC Partition 31..0



MEMORY: FBC Partition 63..32



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PAGE DETAIL	MEMORY: FBC PARTITION[63:32]

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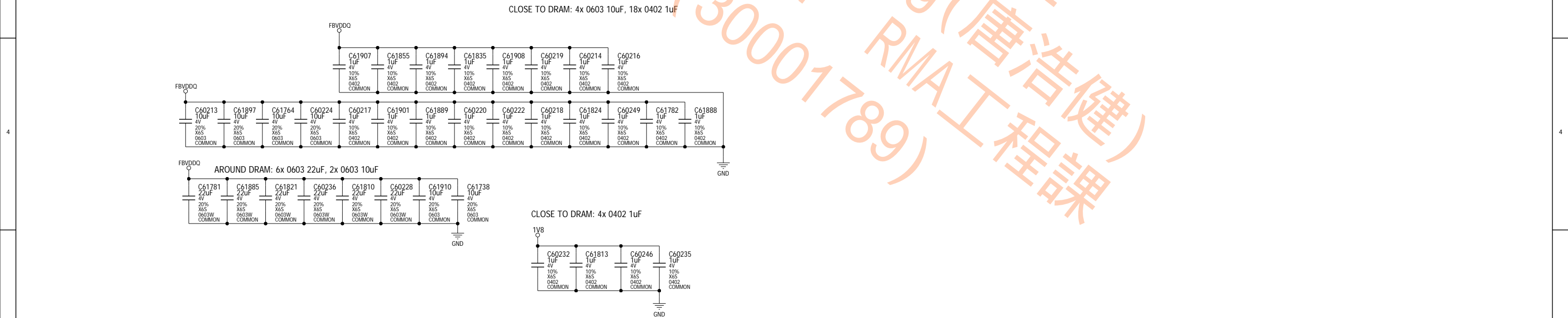
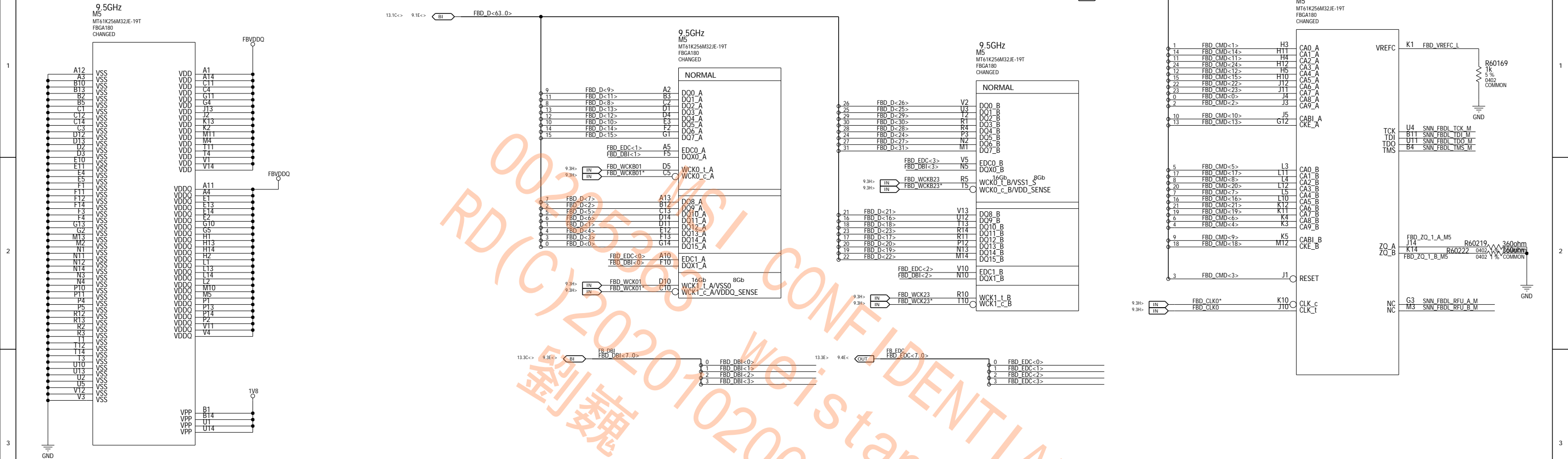
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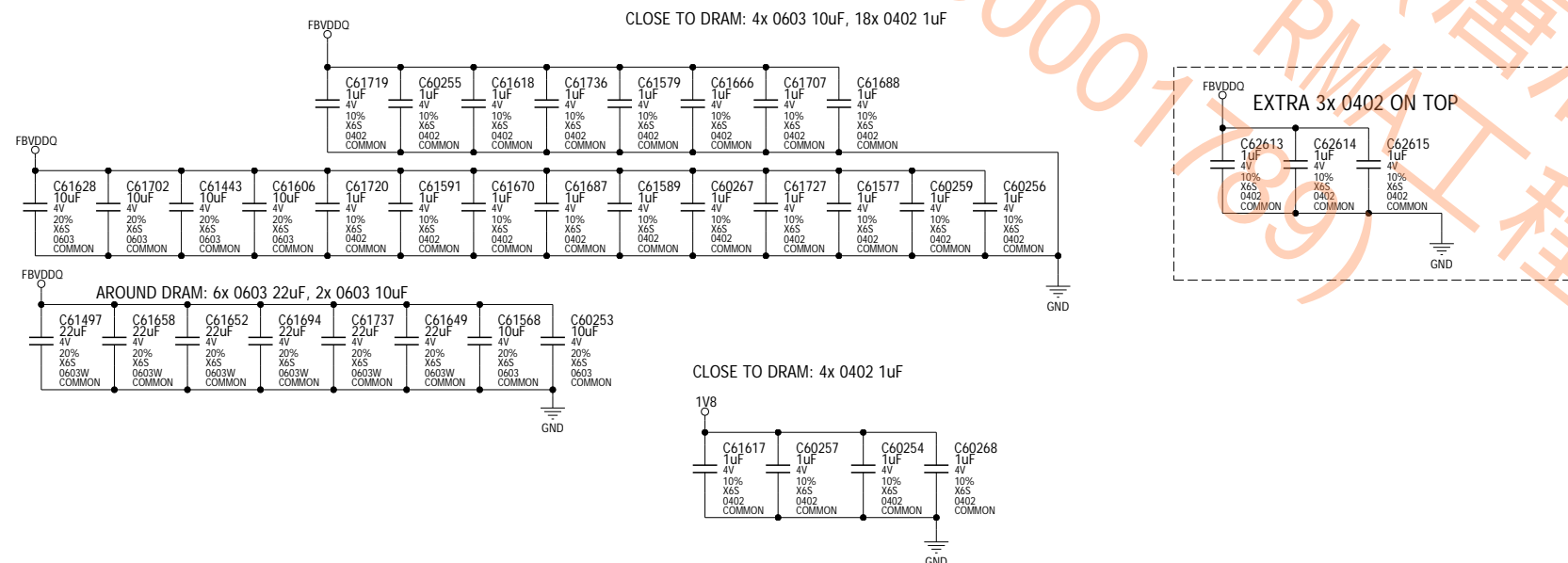
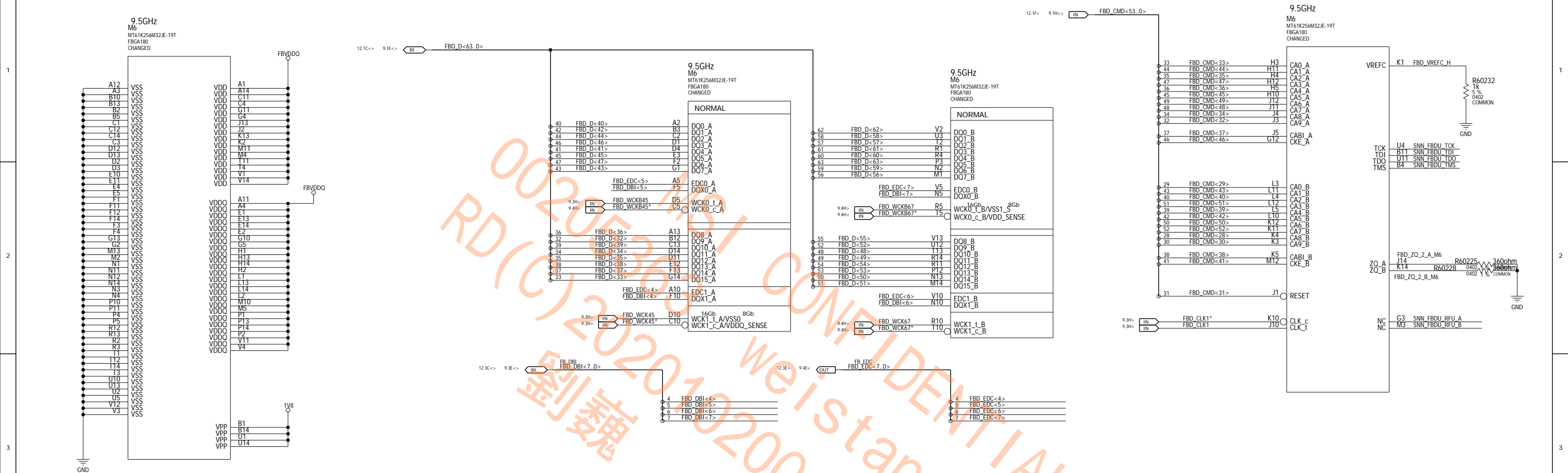





MEMORY: FBD Partition 31..0



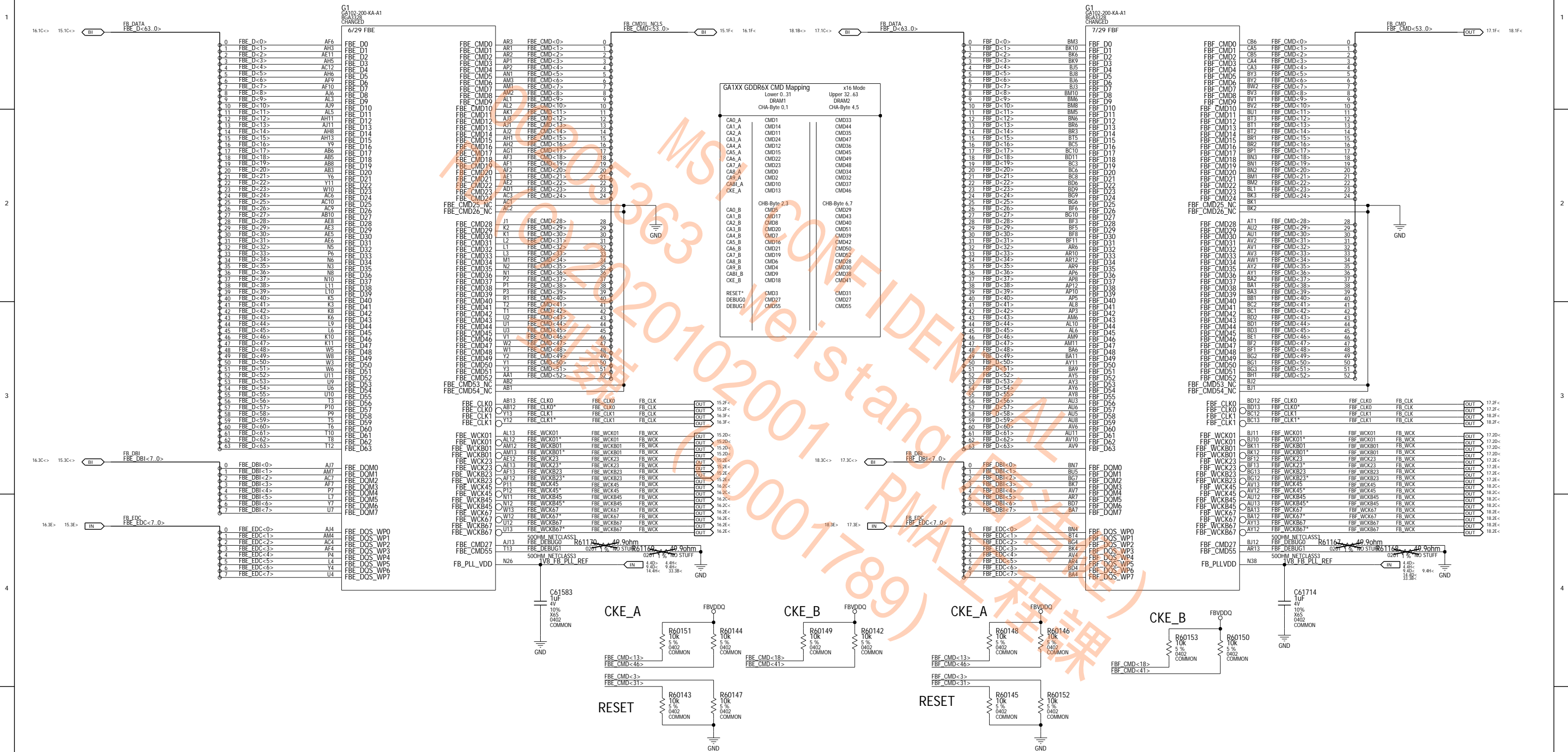
MEMORY: FBD Partition 63..32



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MEMORY: GPU Partition E/F



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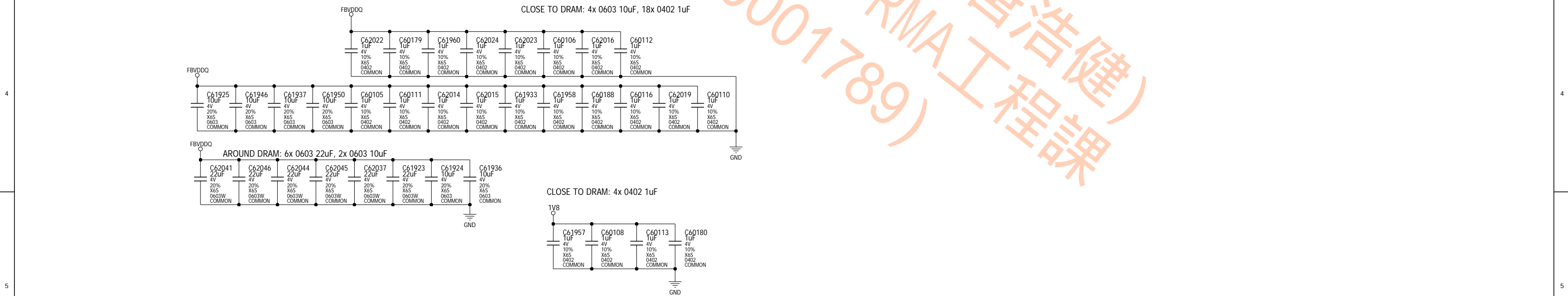
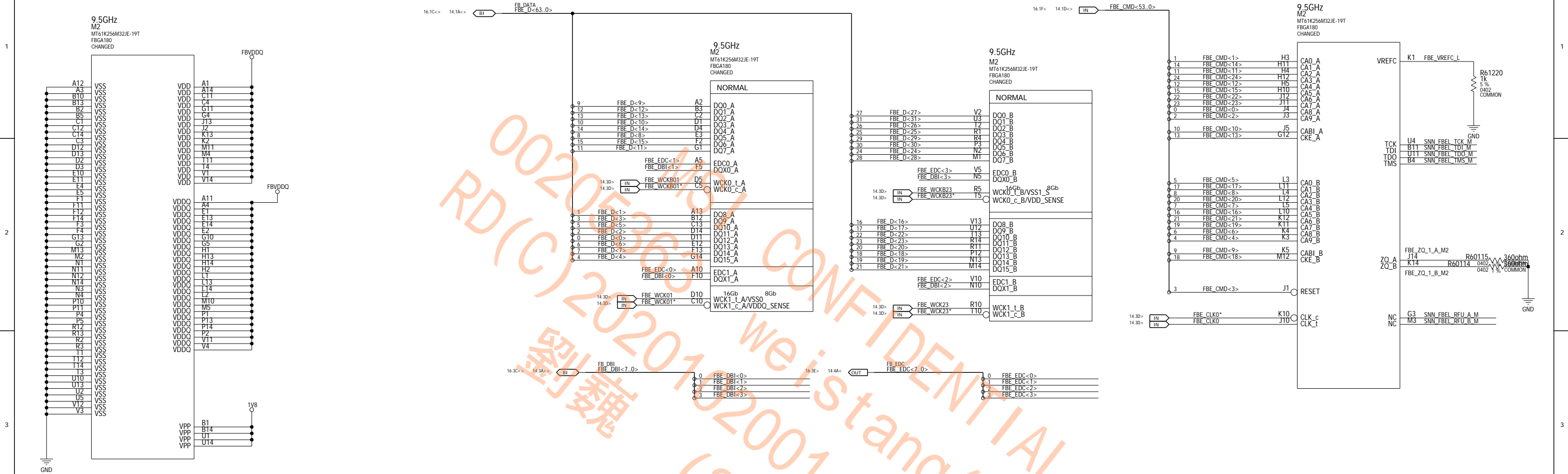
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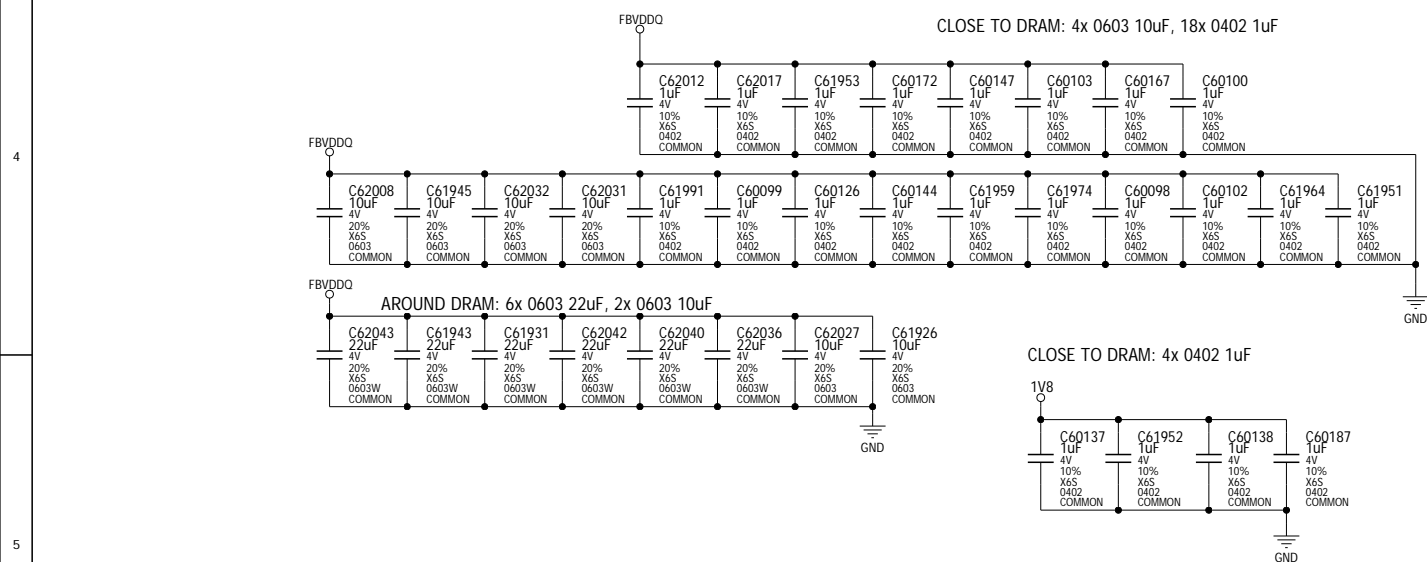
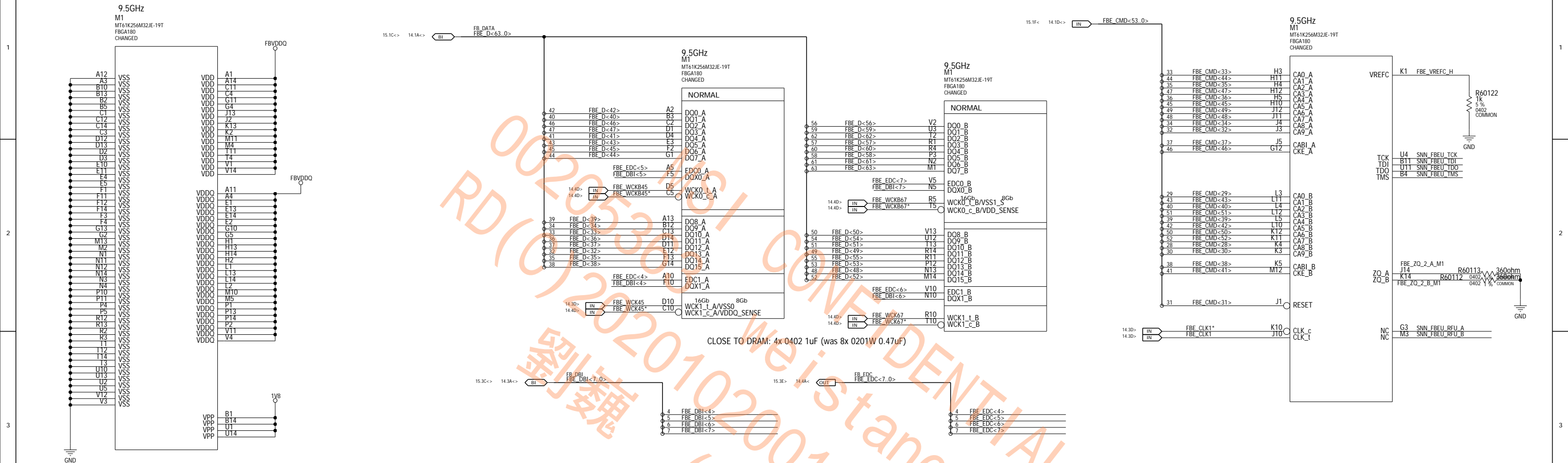
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MEMORY: FBE Partition 31..0



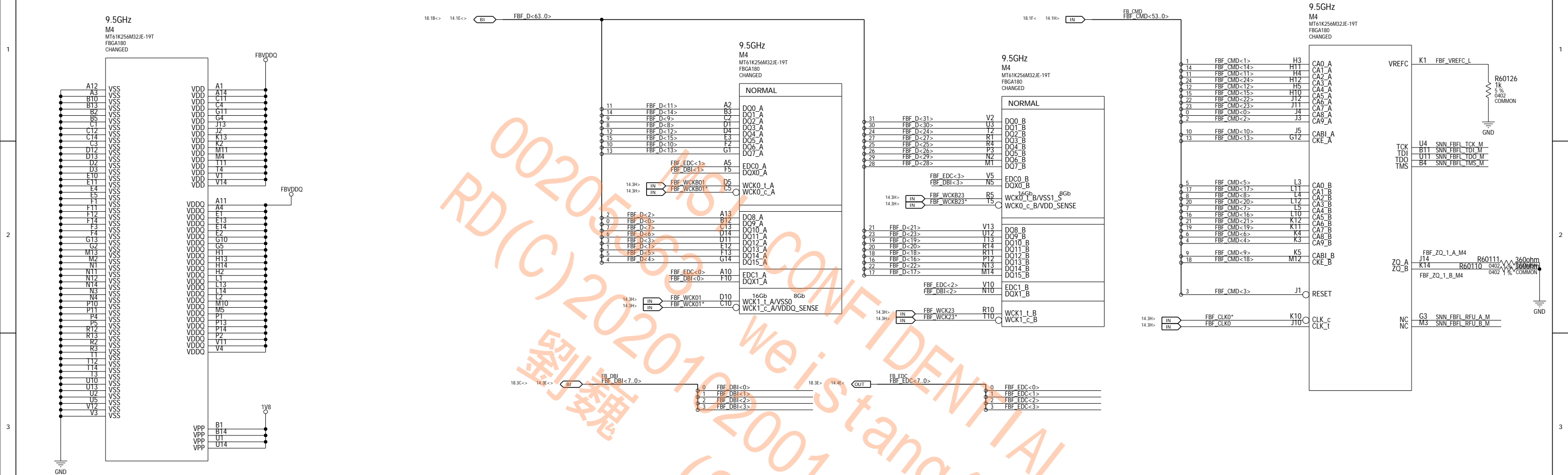
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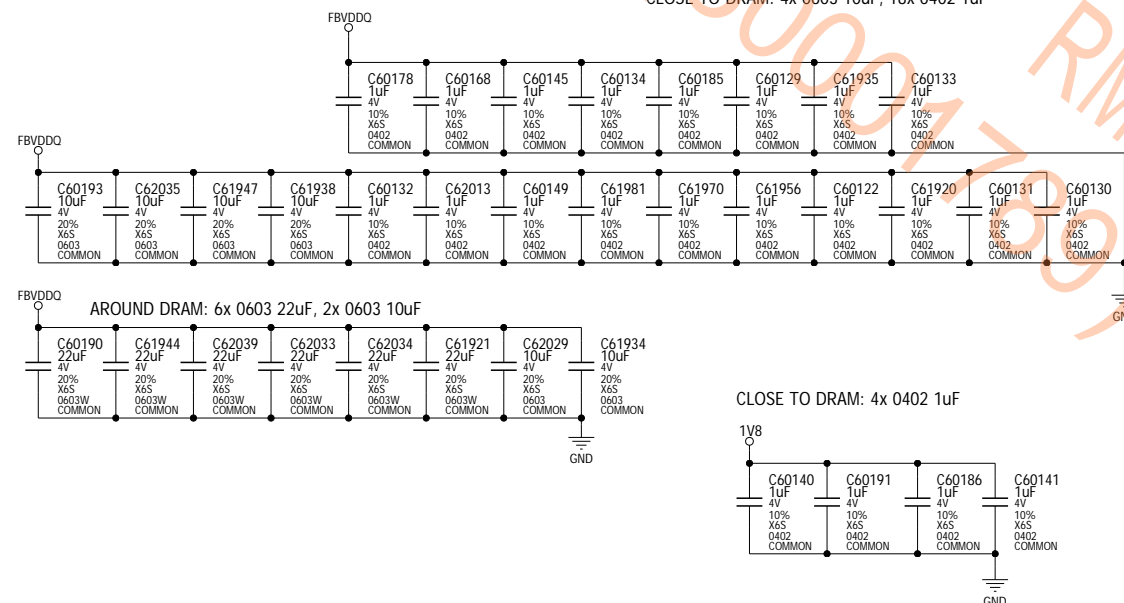
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MEMORY: FBF Partition 31..0



CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF

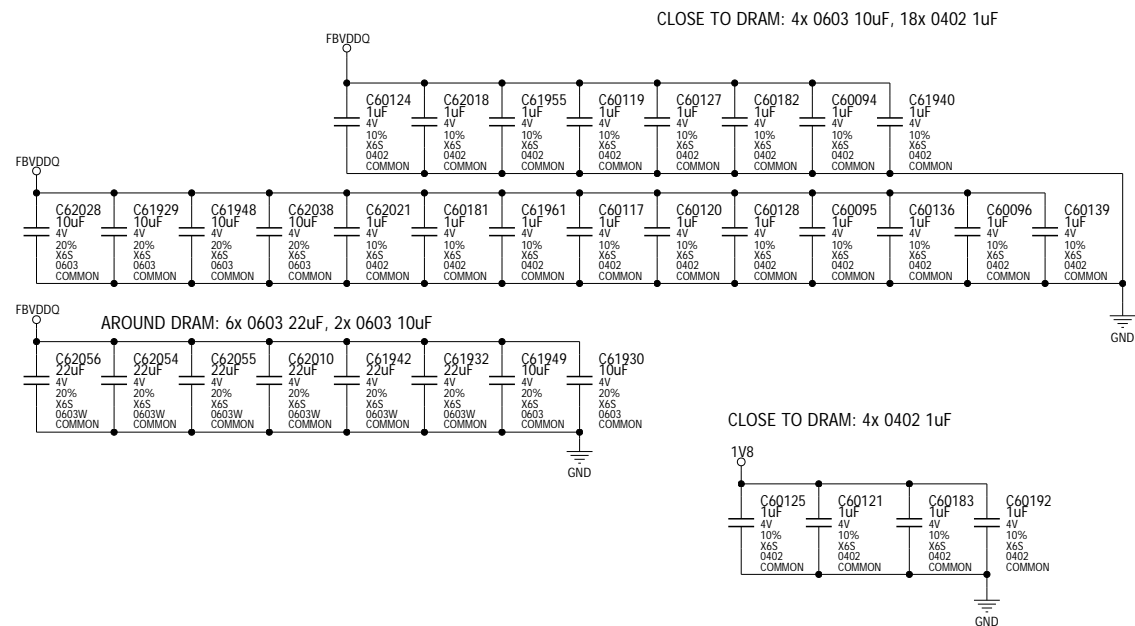
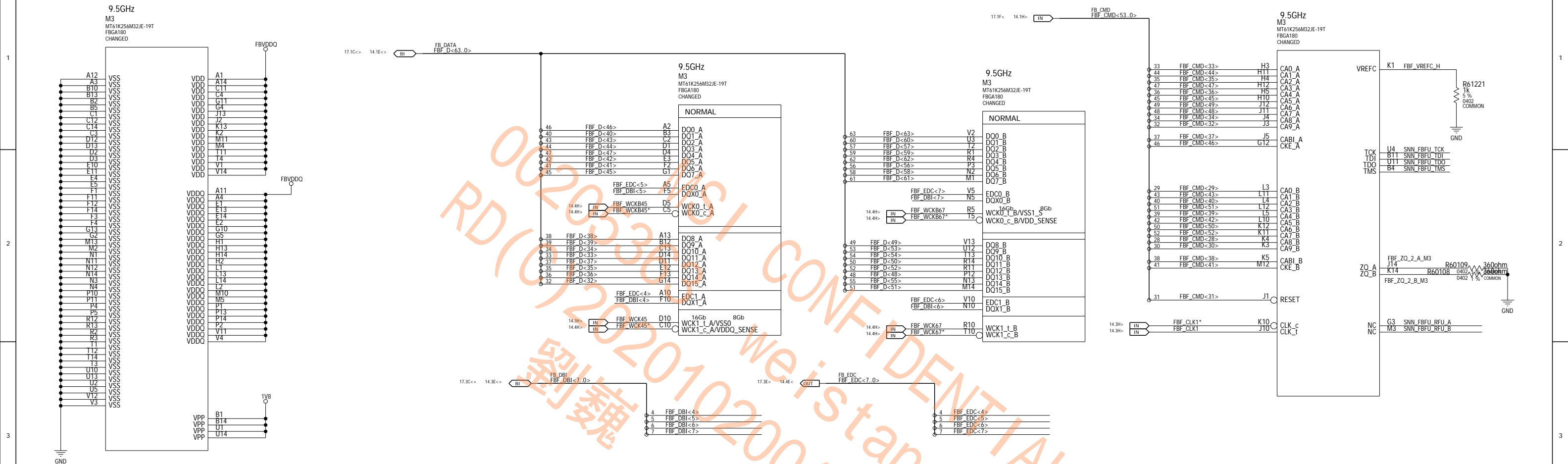


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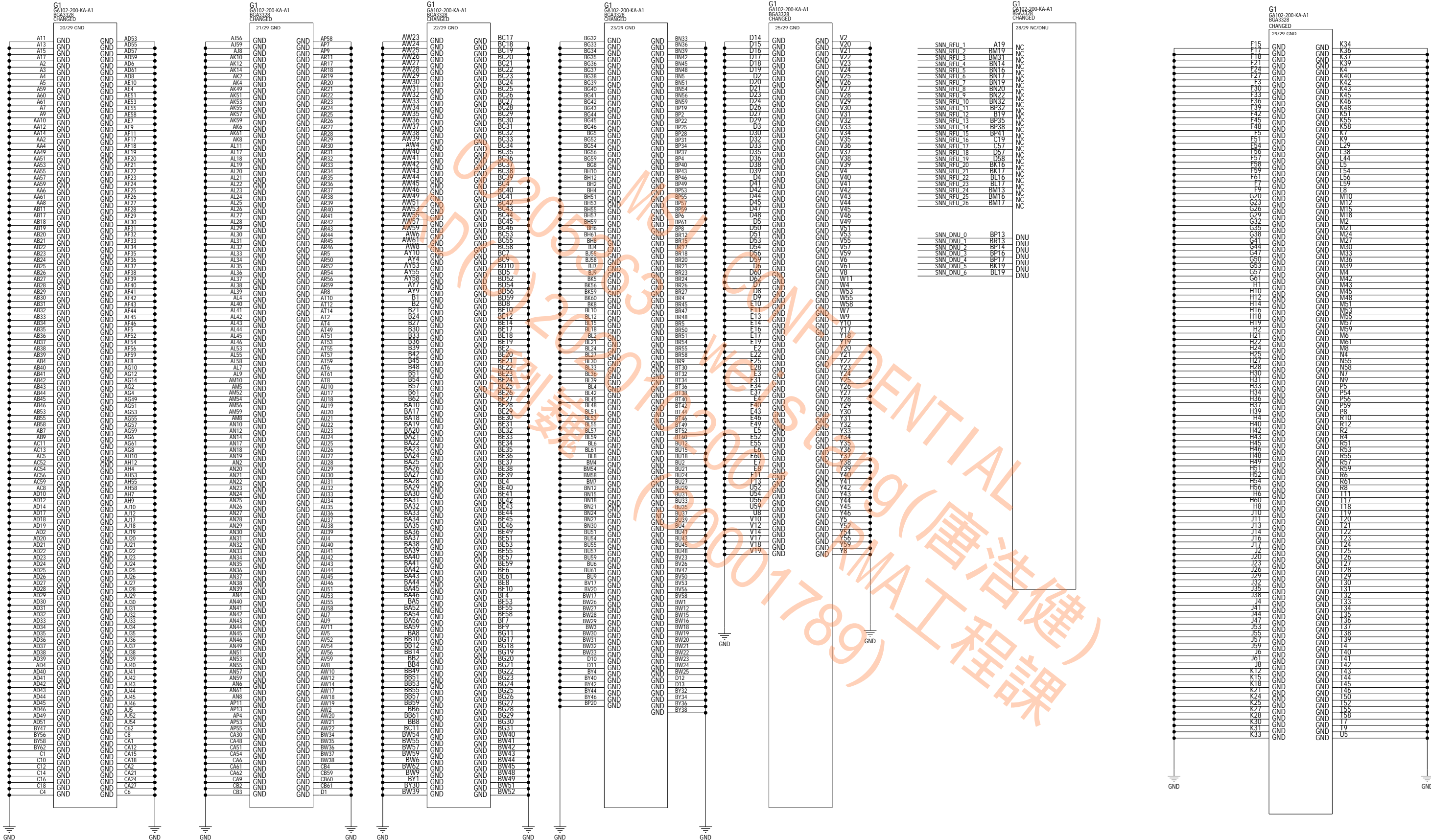
MEMORY: FBF Partition 63..32



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PAGE DETAIL	MEMORY: FBF PARTITION[63:32]

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GPU GND, RFUs & RSVD



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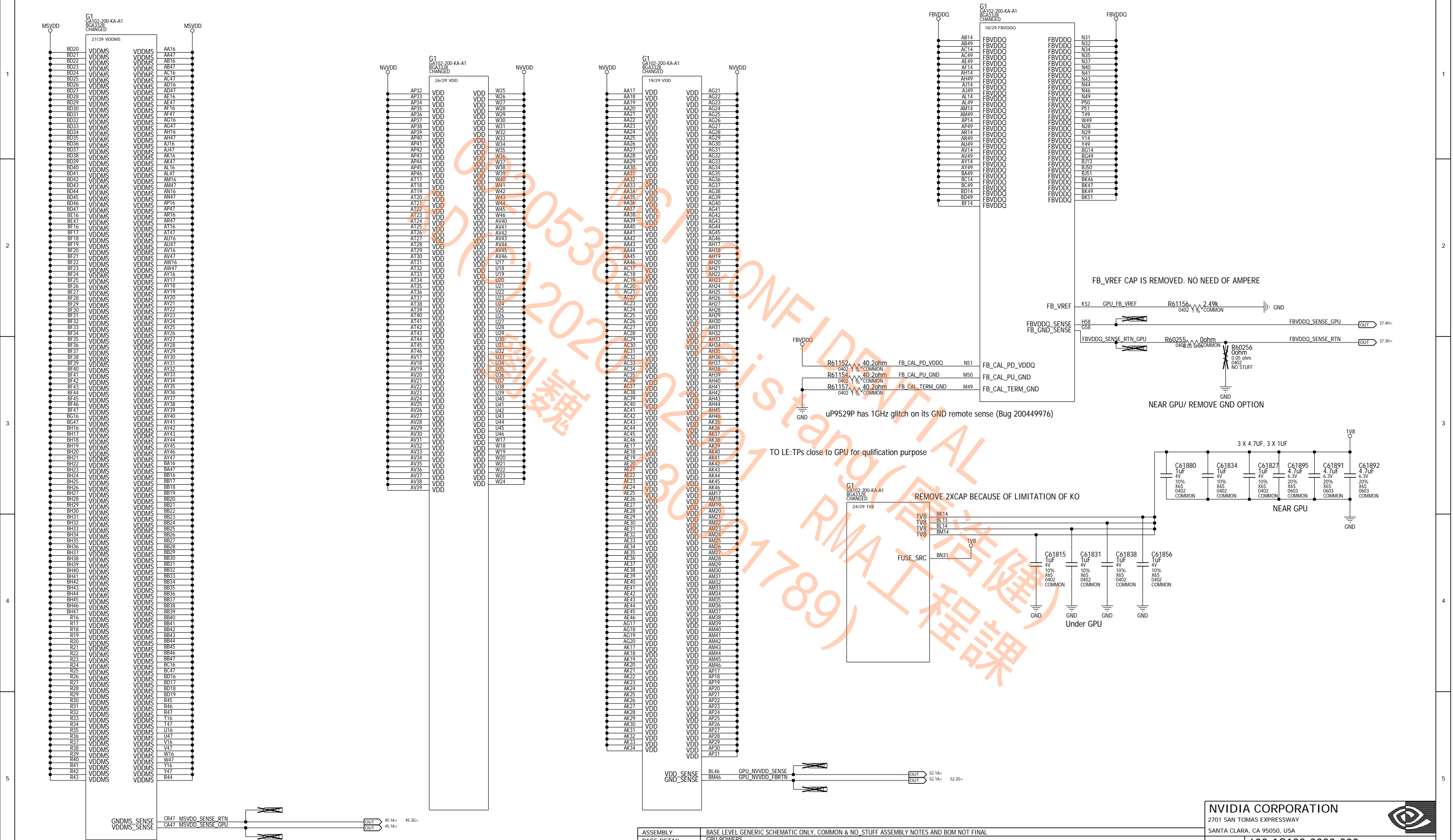
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PAGE DETAIL	GPU GND, RFUS & RSVD

## GPU PWR and GND



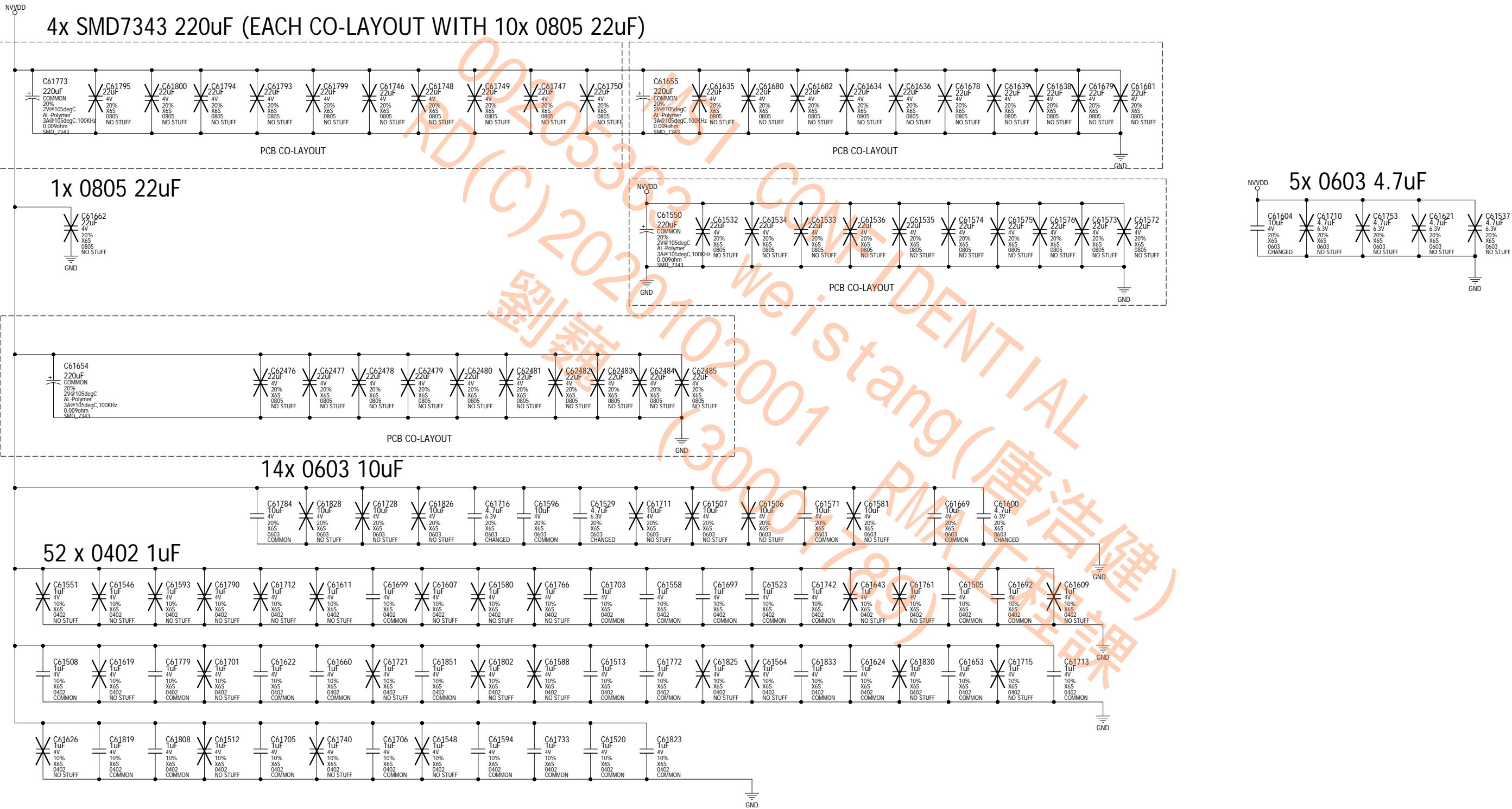
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	GPU POWERS

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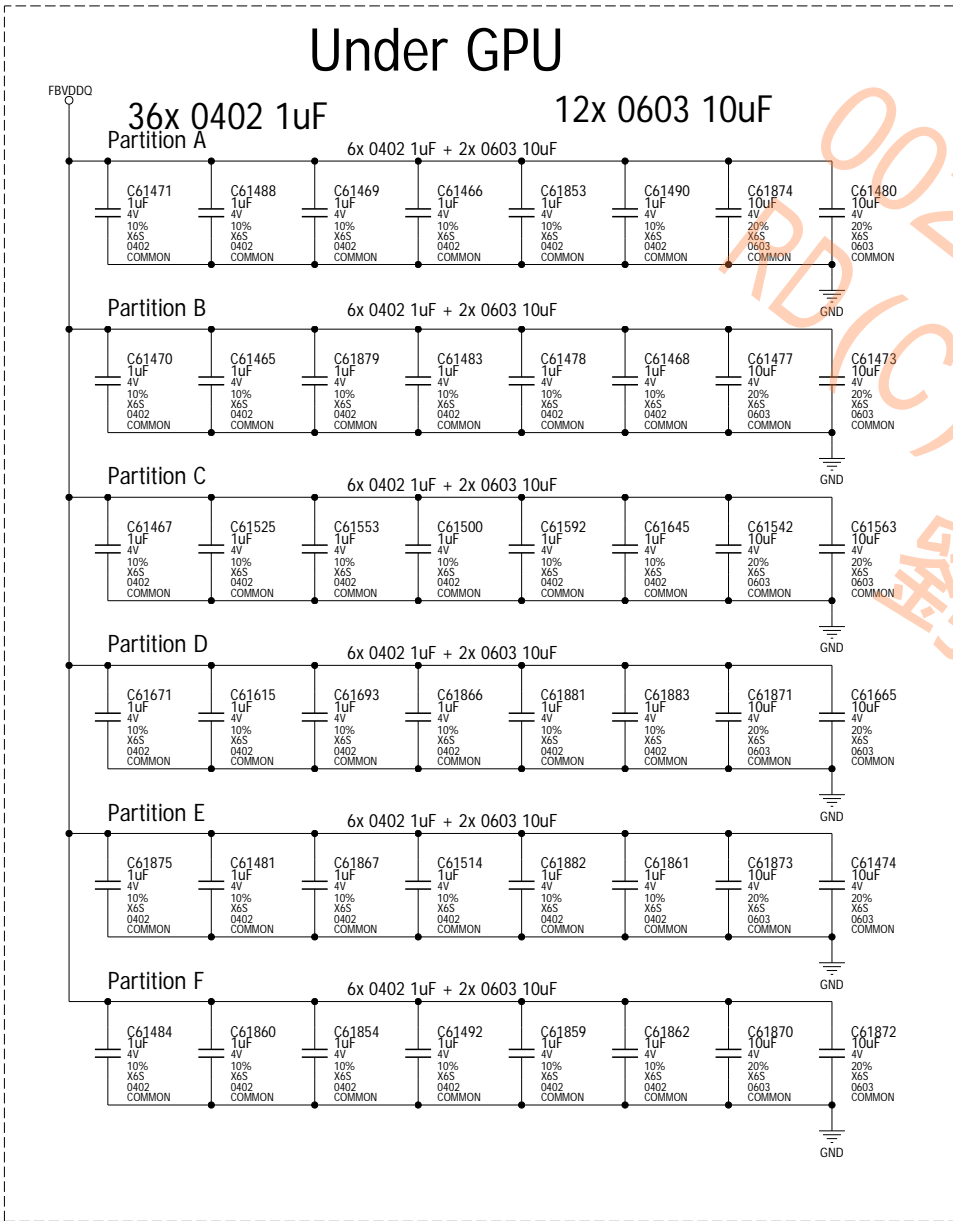
# NVVDD UNDER GPU



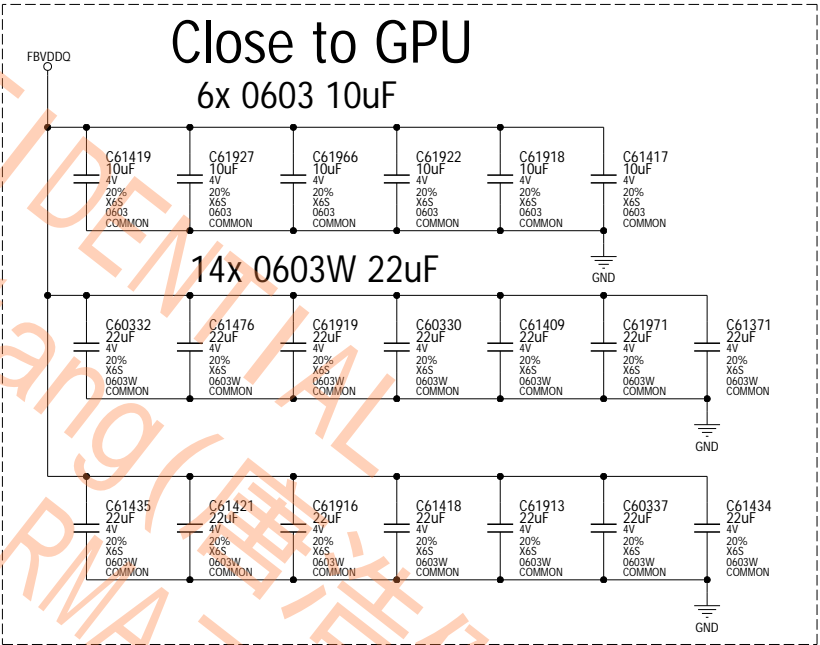
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FBVDDQ

Under GPU

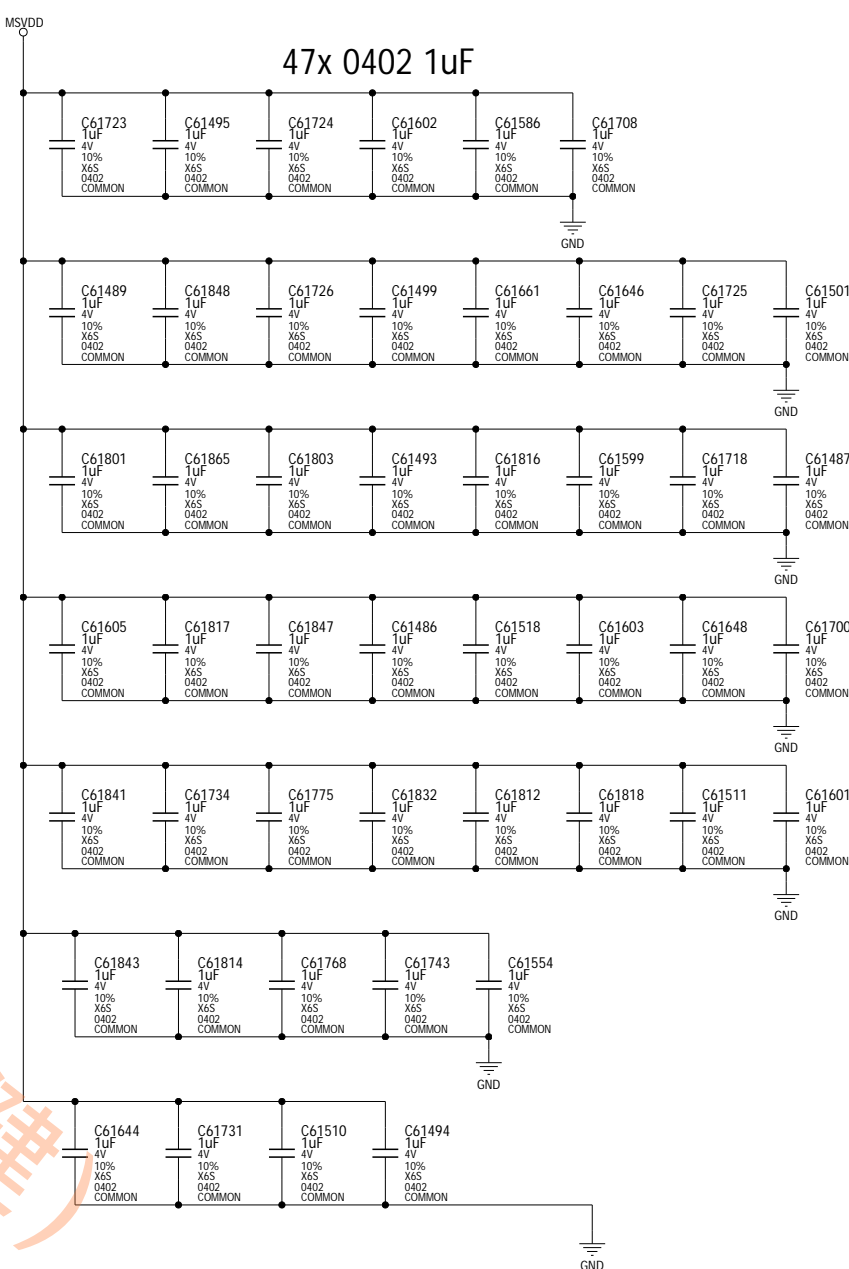
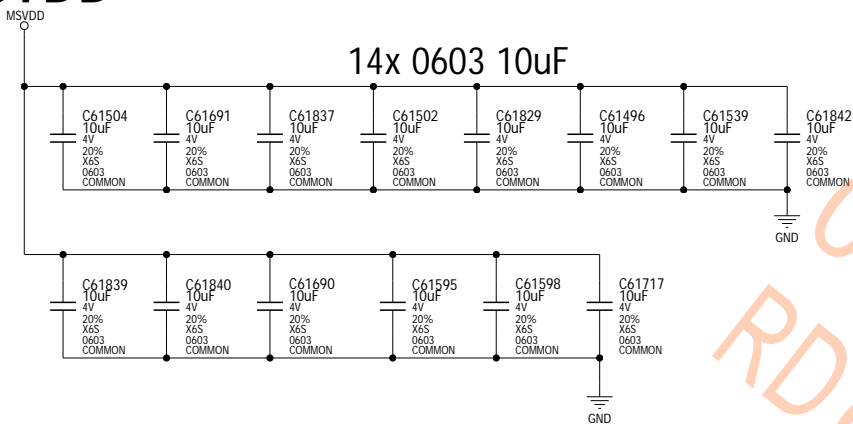


Close to GPU

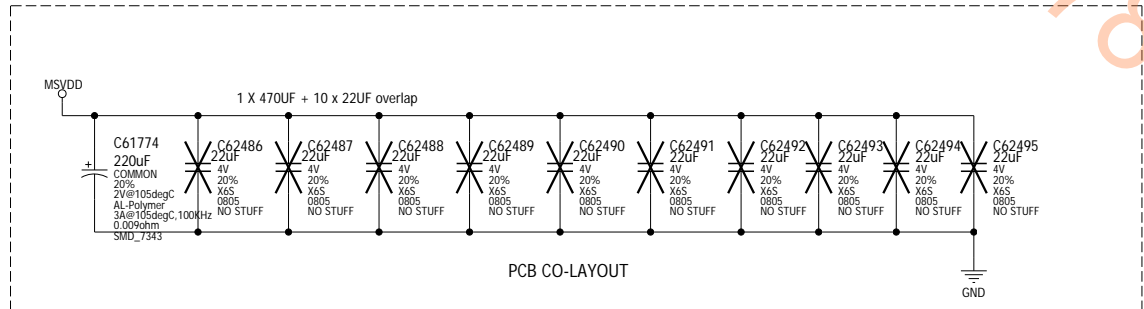
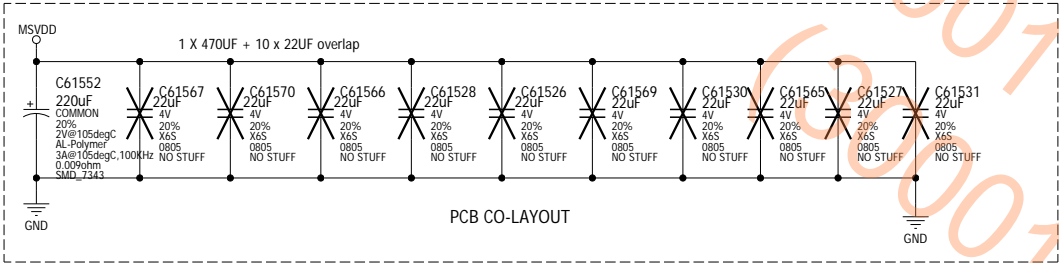


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# UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

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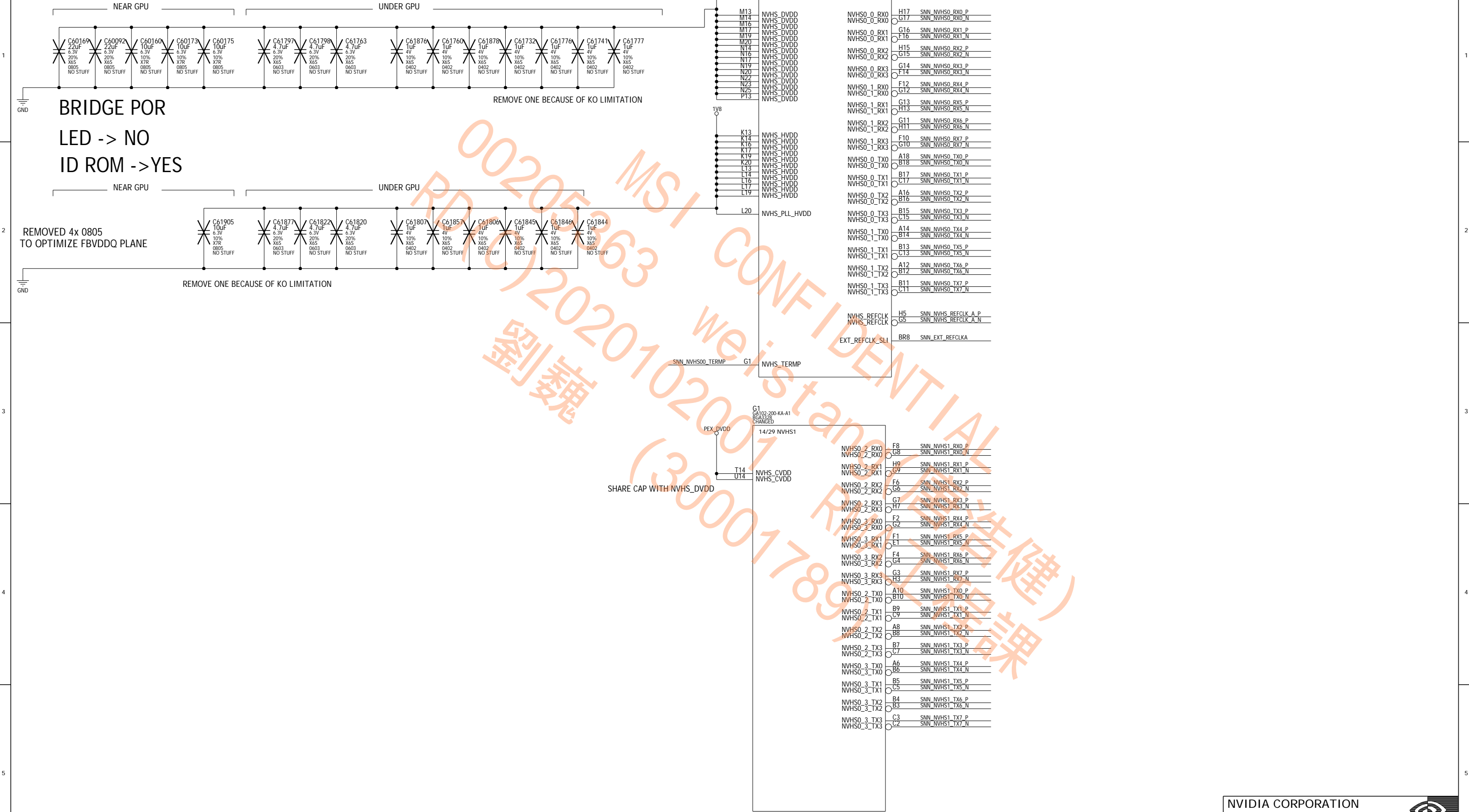
SANTA CLARA, CA 95050, USA



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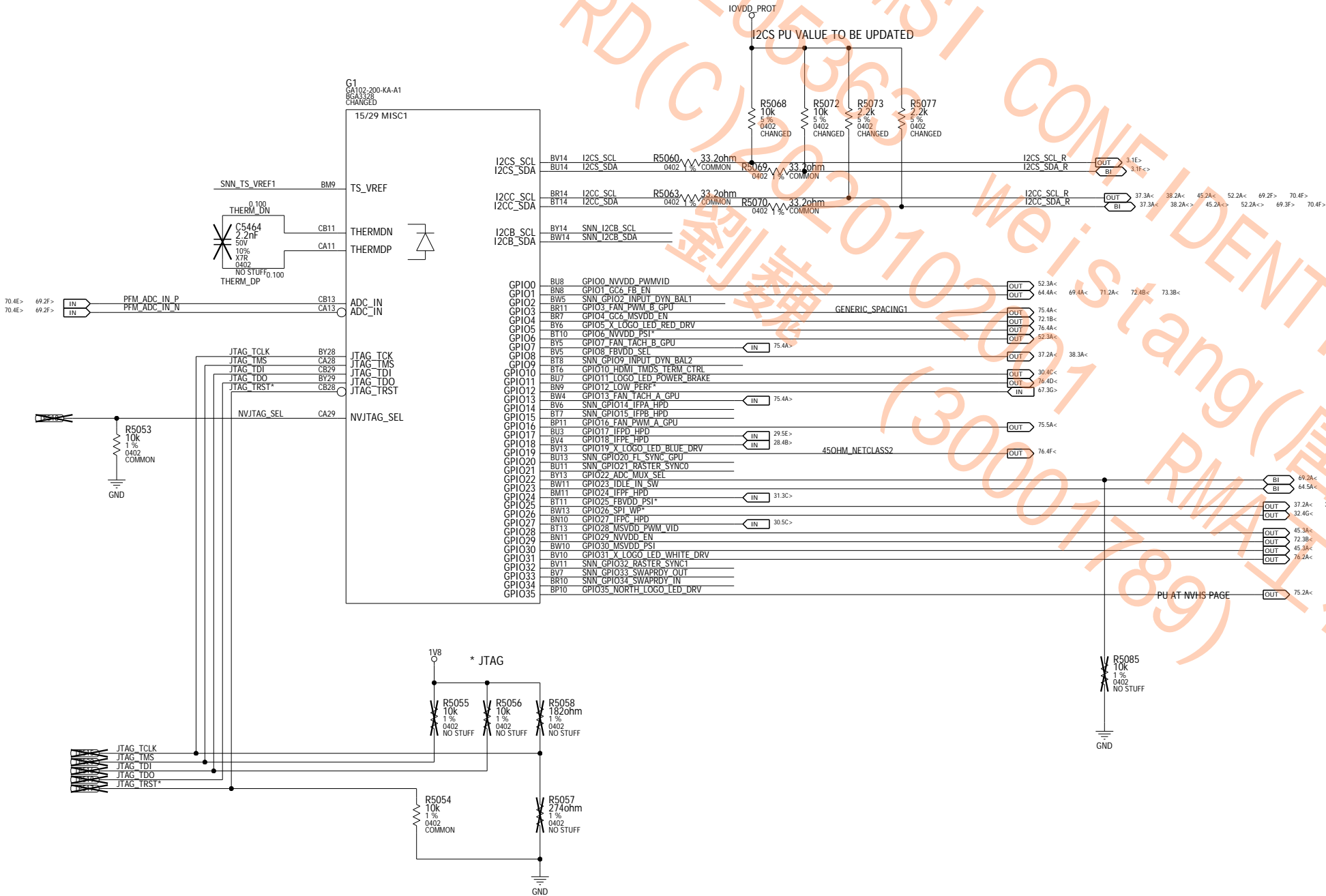


NVHS Interface and FRAME LOCK



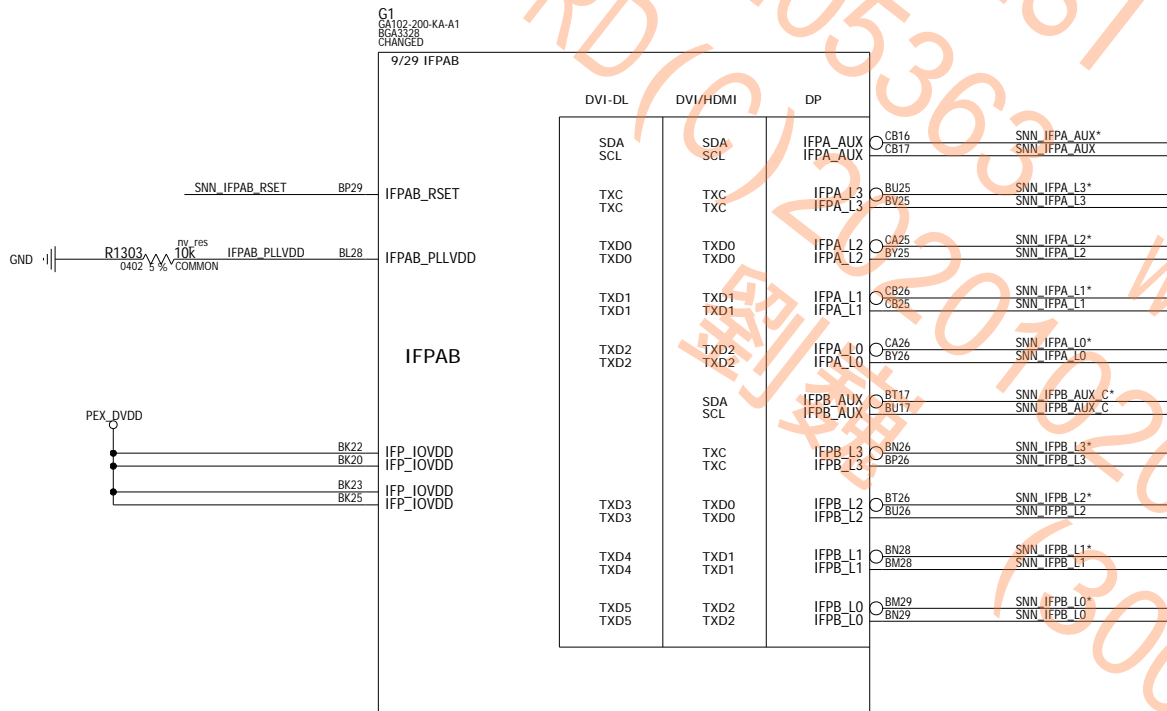
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MISC1: Fan, Thermal, JTAG, GPIO, STEREO



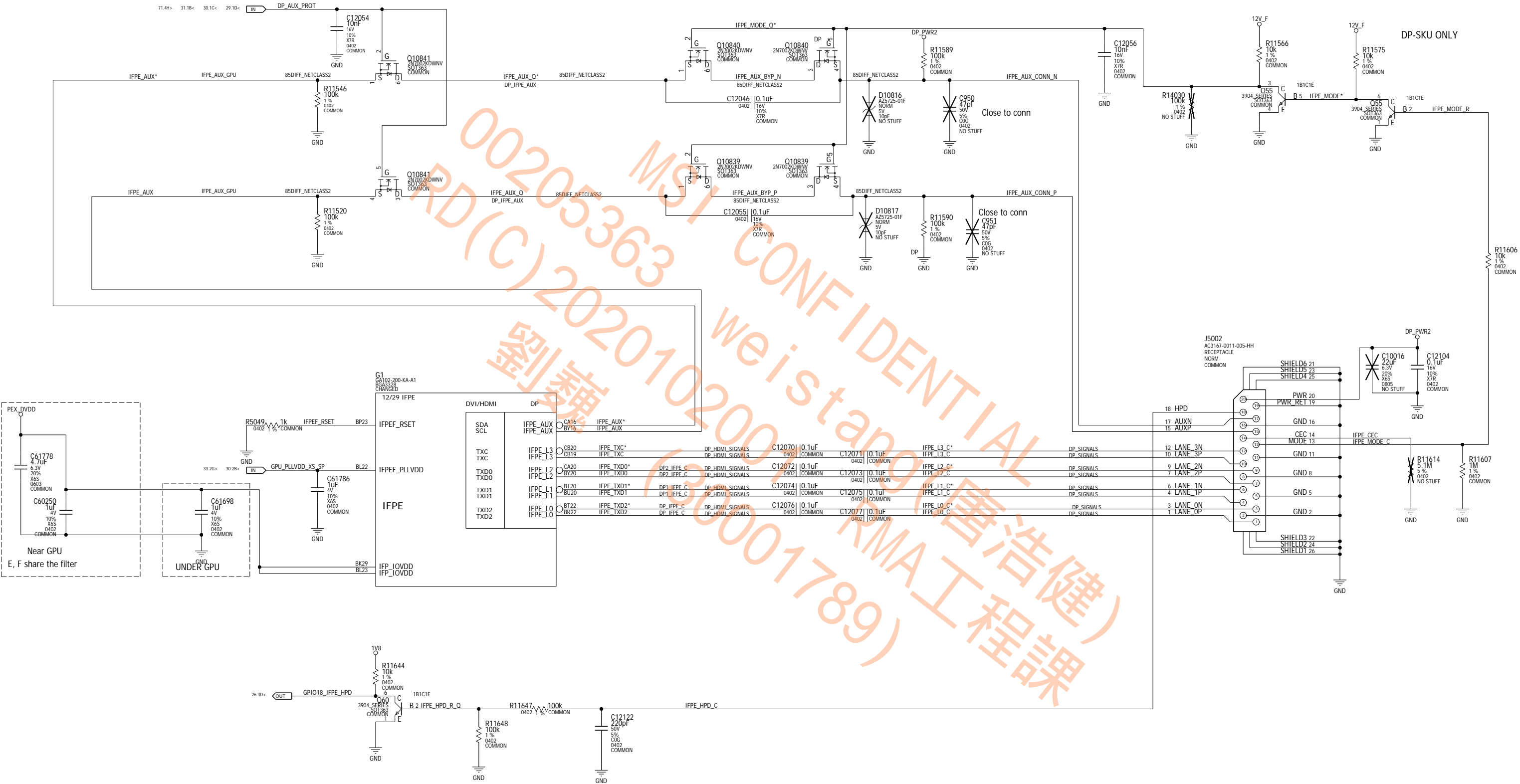
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IFPA UNUSED, IFPB UNUSED



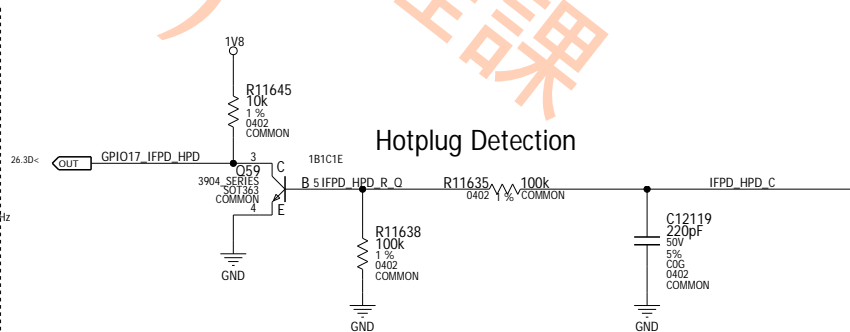
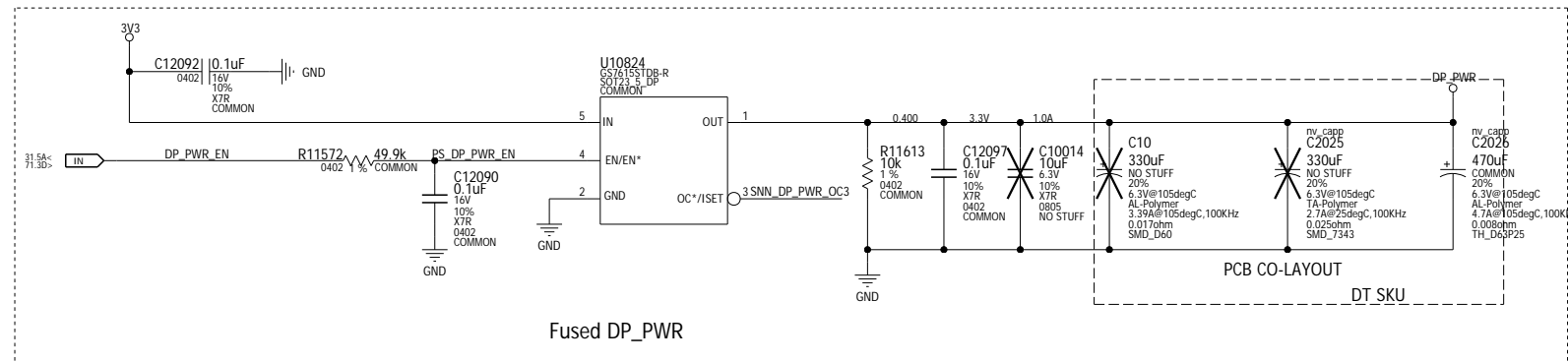
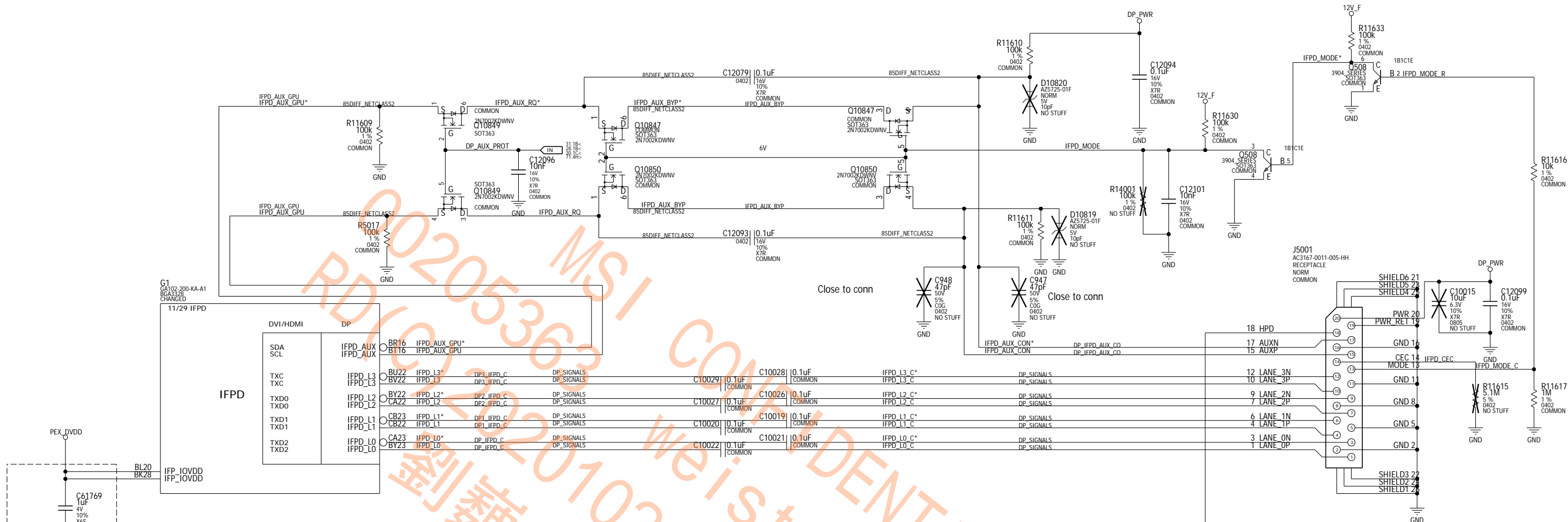
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IFPE DP





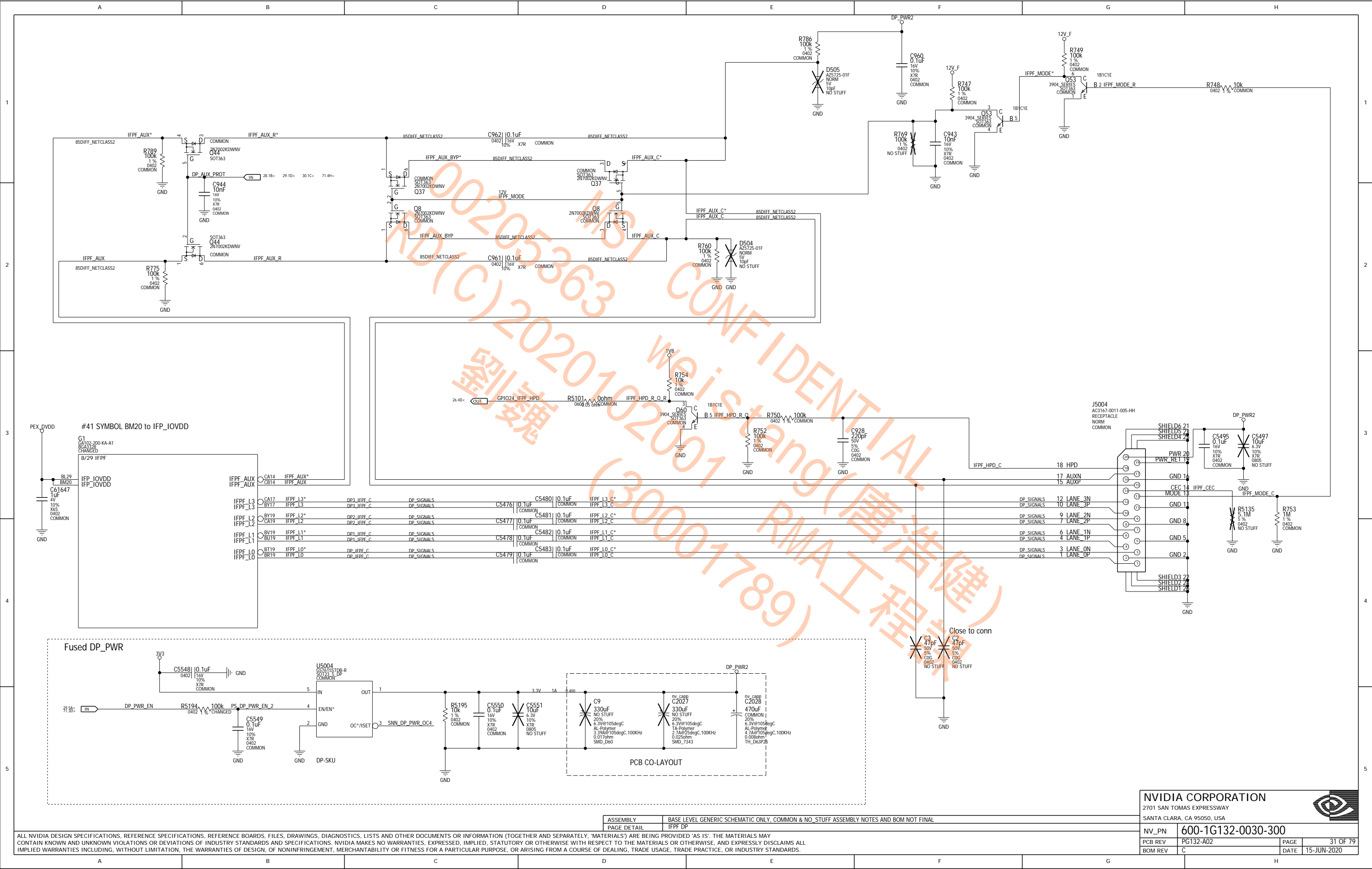
## IFPD DP



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPF DP

MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
H	H	H	0111	FS_OVERT ENABLE	
L	L	L	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

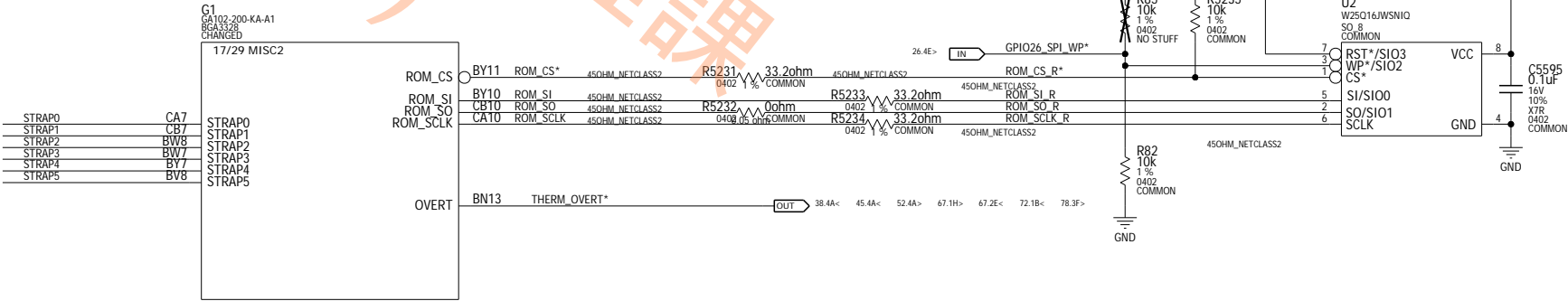
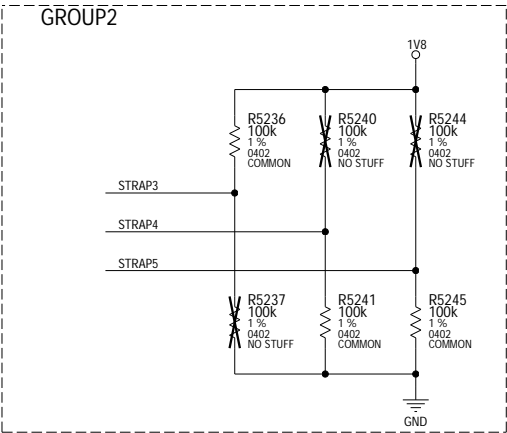
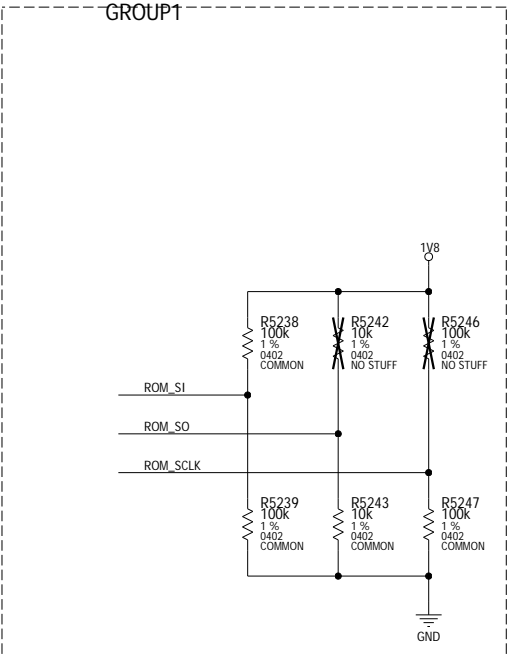
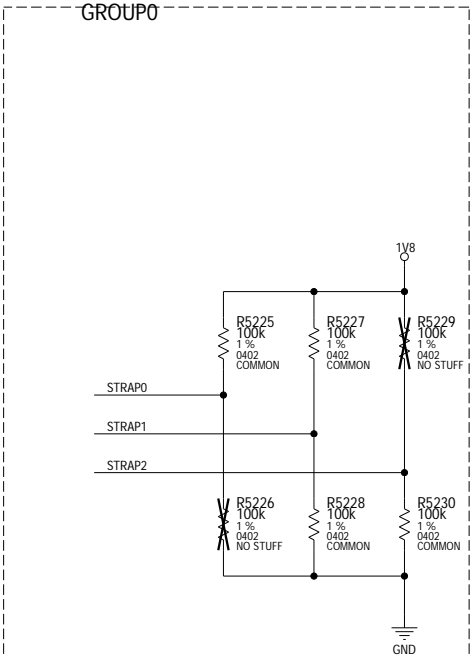
Default

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

<-A01 PCB

<-OLD

<-LATEST A02 PCB



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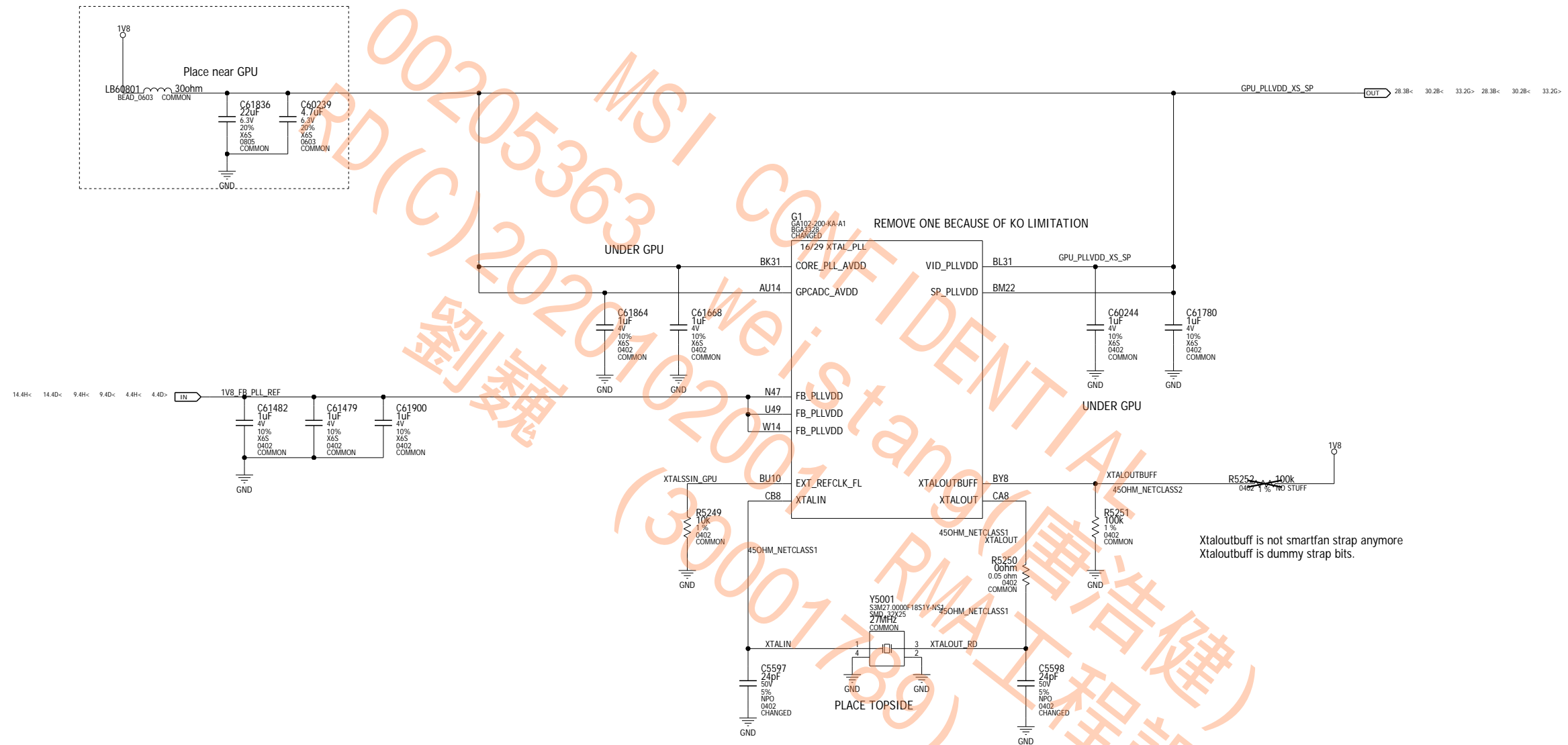
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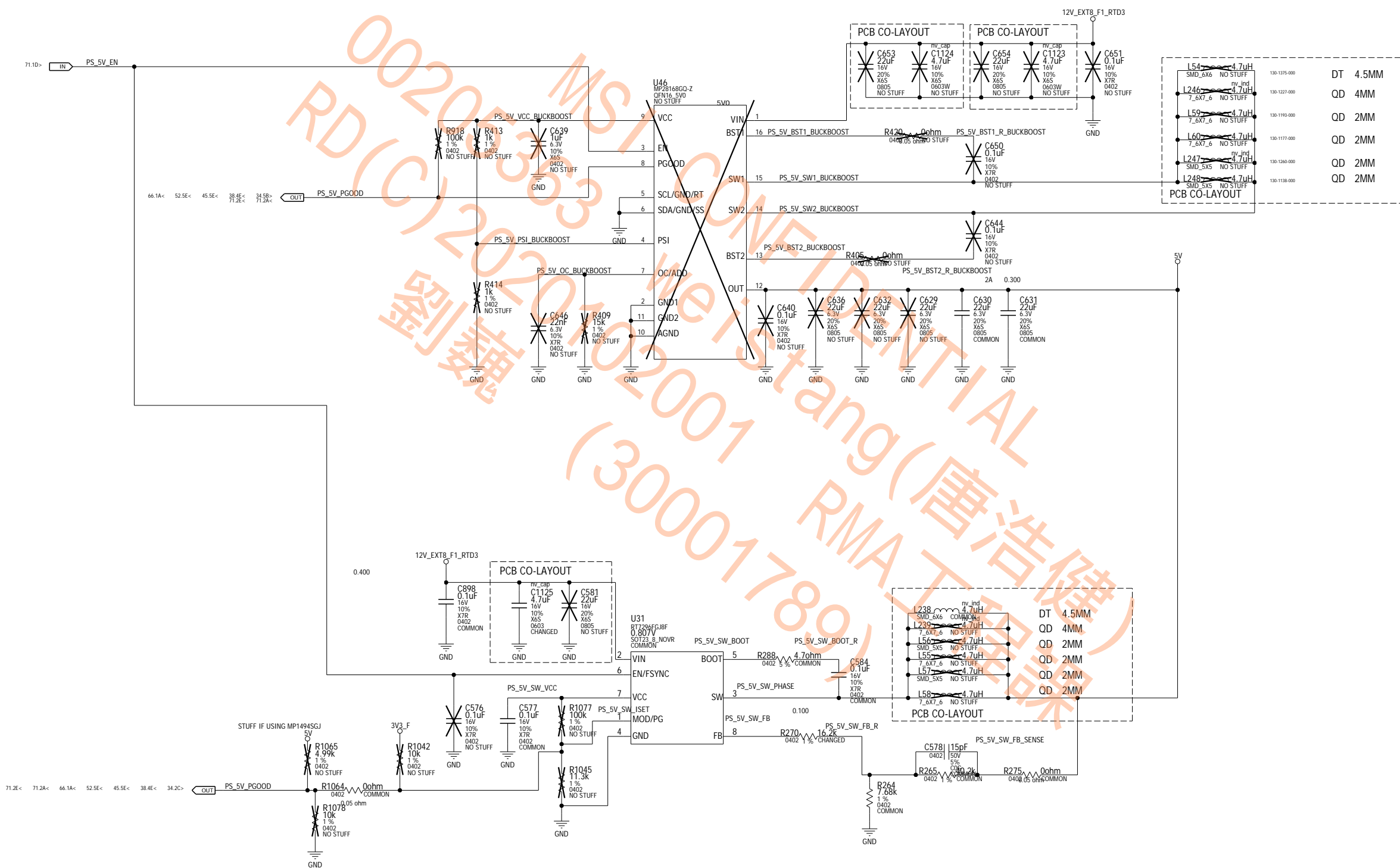
## MISC: XTAL. PLL



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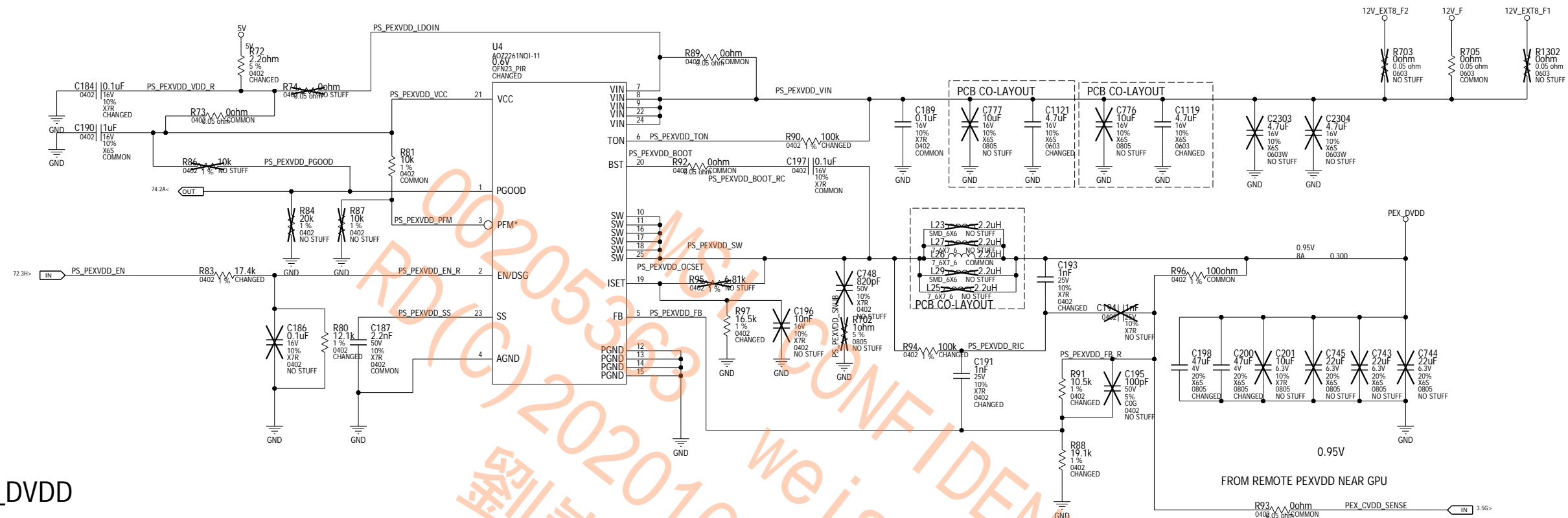
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PS: 5V, 5V\_BACKUP

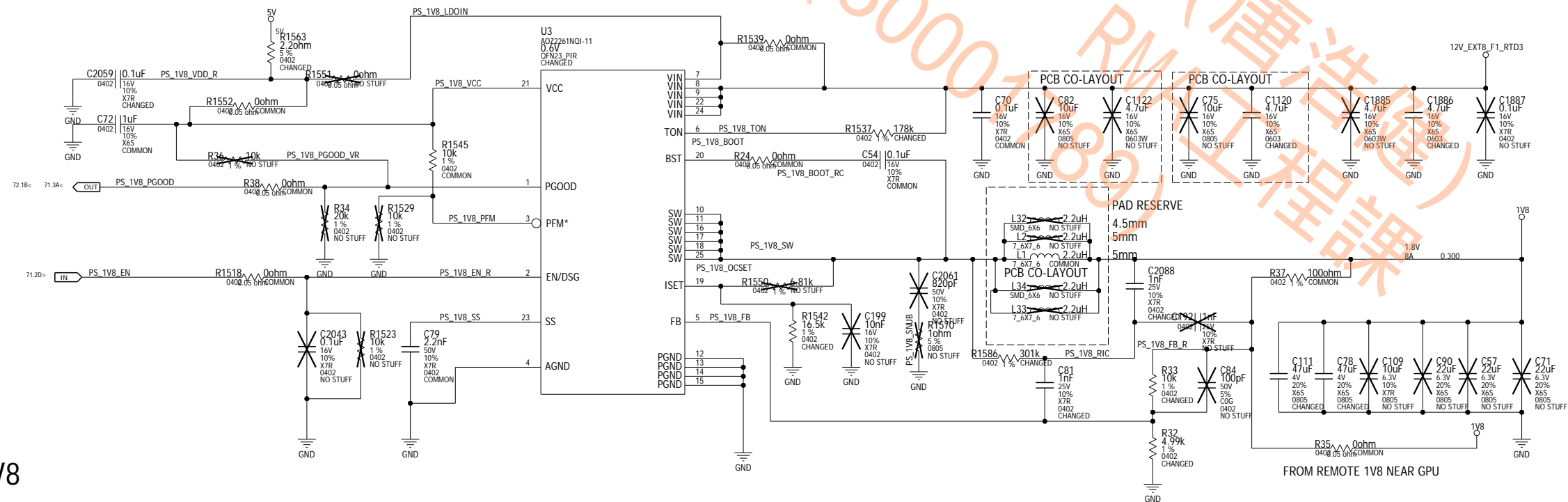


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PS: PEX\_DVDD 1V8 Rail



PEX\_DVDD



1V8

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PAGE DETAIL	PS: PEX_DVDD and 1V8

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(30001789) RMA工程課


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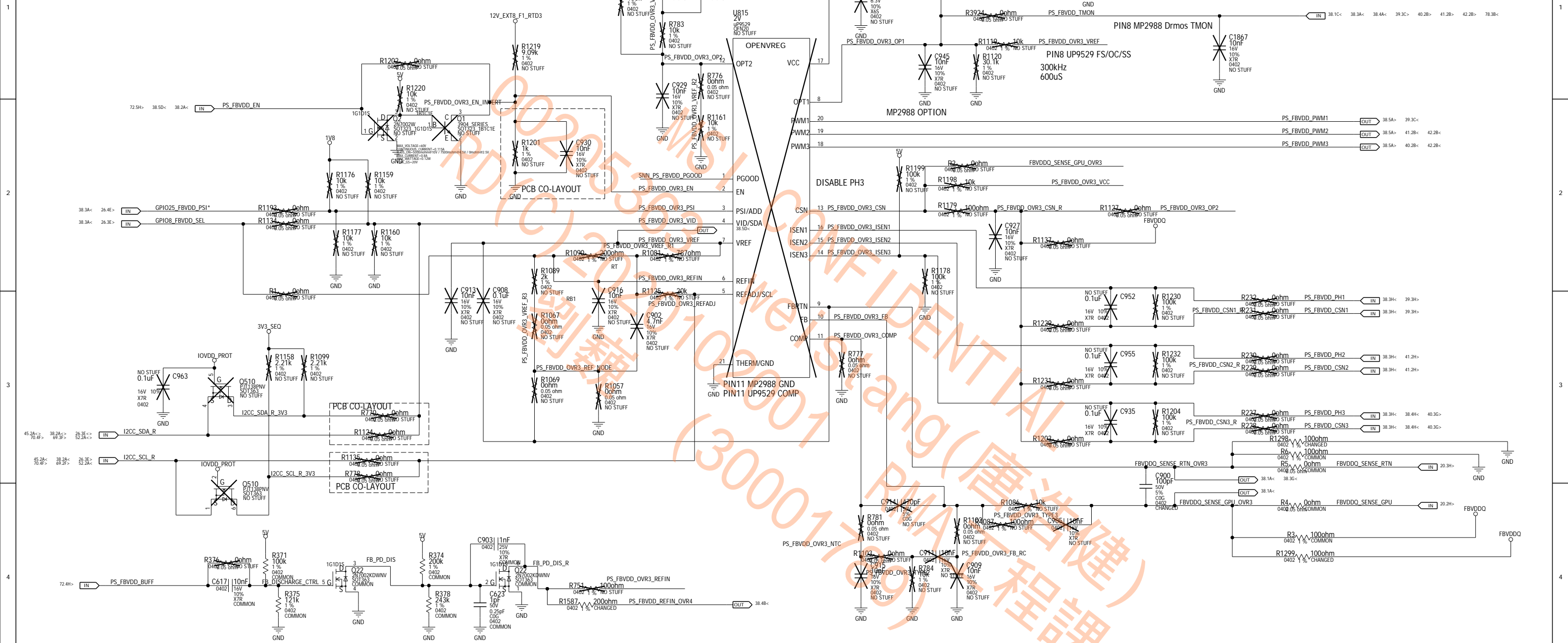
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## PS: FBVDD Controller OVR3

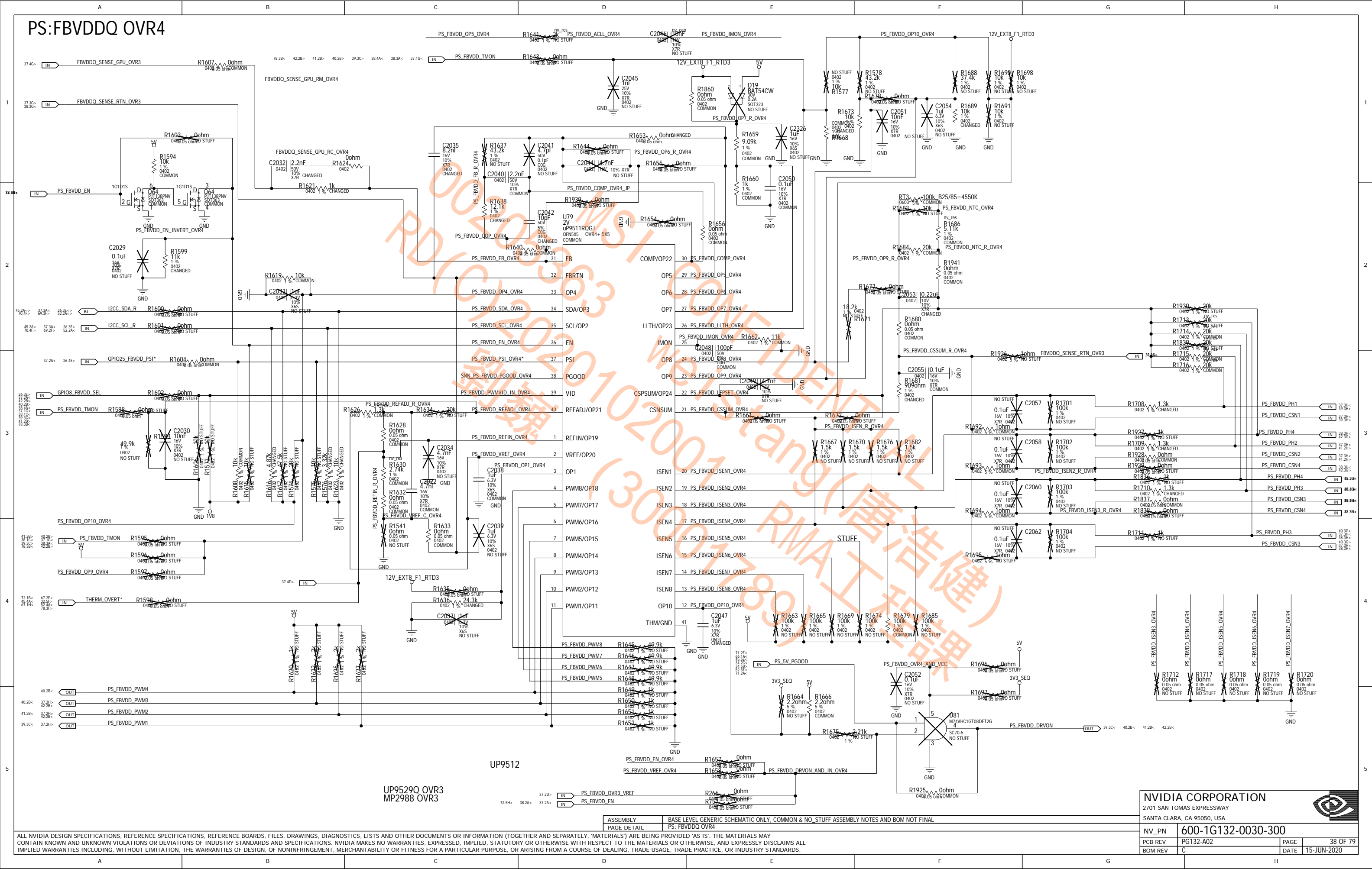
PIN12 MP2988 VIN SENSE 1/16 DIVIDER  
PIN12 UP9529 REFOUT

FOR DT SKU

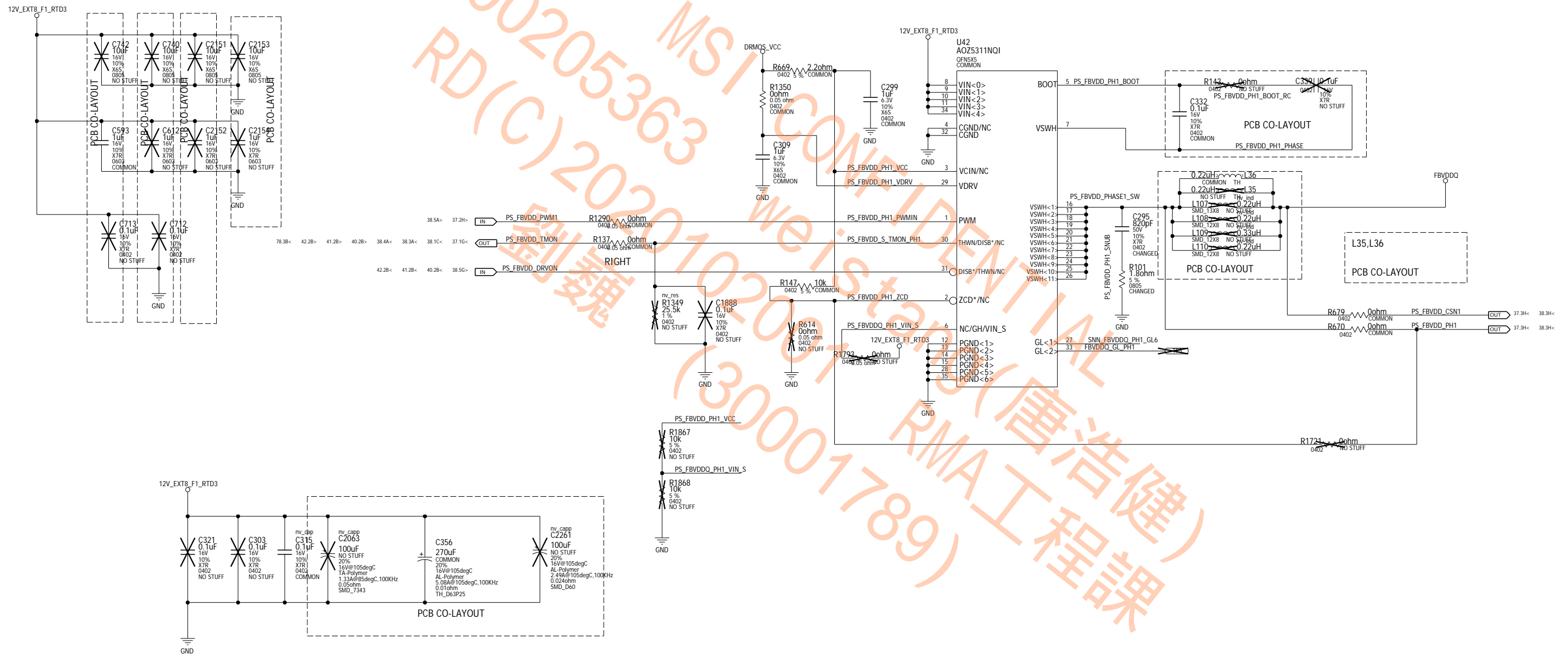
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<b>PCB REV</b>		<b>PG132-A02</b>		<b>PAGE</b> 37 OF 79
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PS:FBVDDQ OVR4



## PS: FBVDD PH1

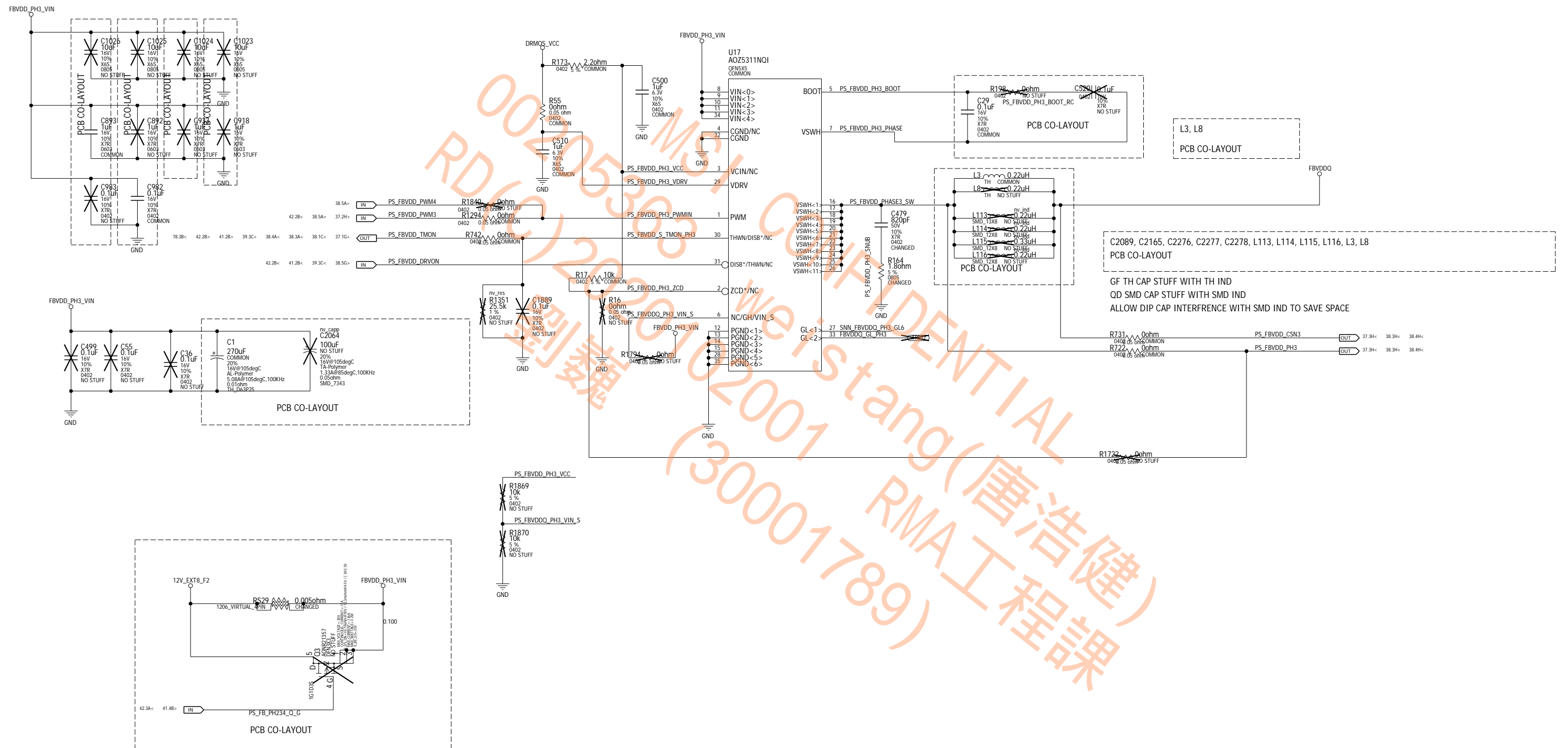


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## PS: FBVDD PH3



### FBVDD PH3 INPUT ANTI-BACKDRIVE

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PAGE DETAIL	PS: FBVDD PH3

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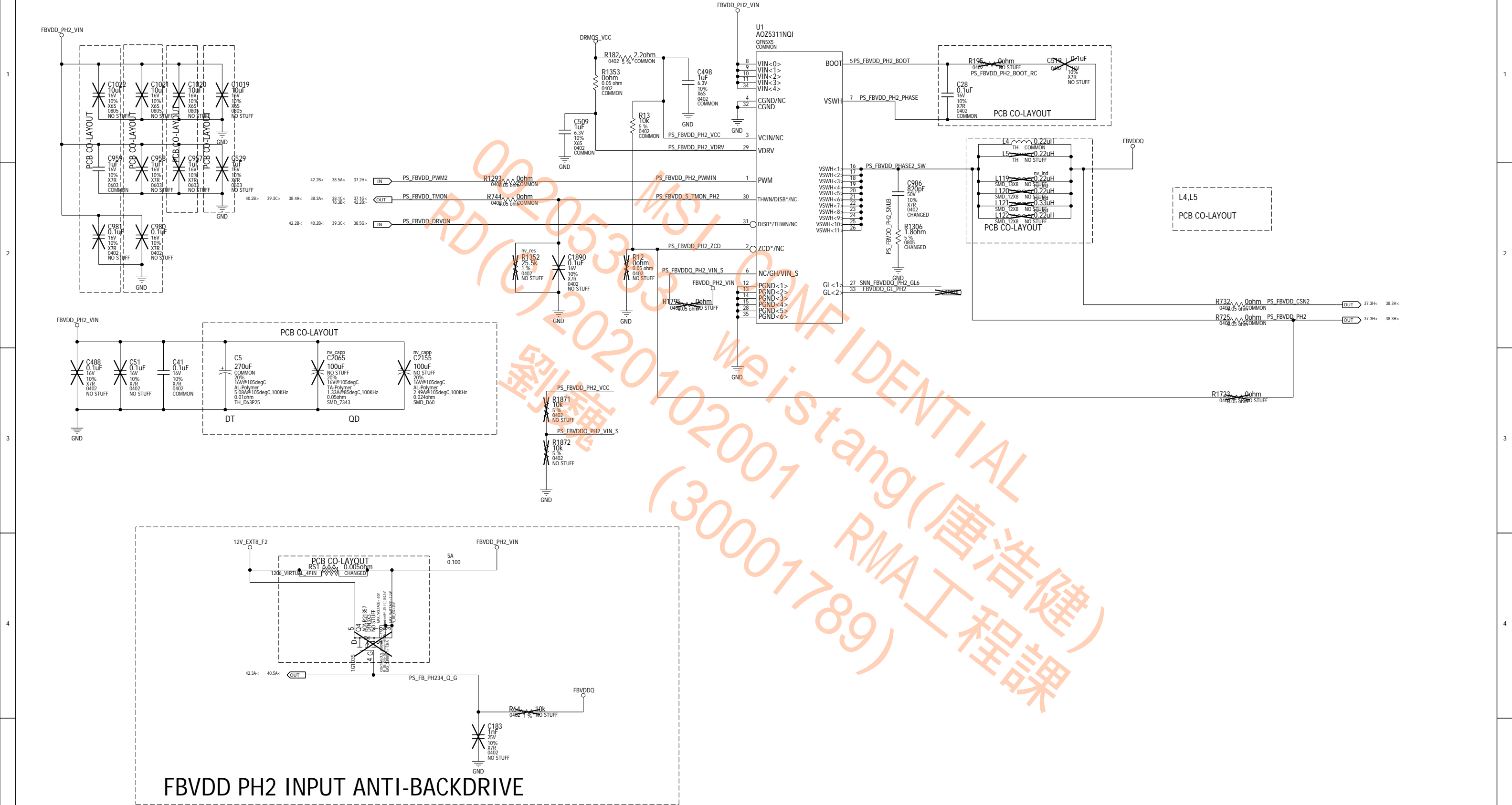
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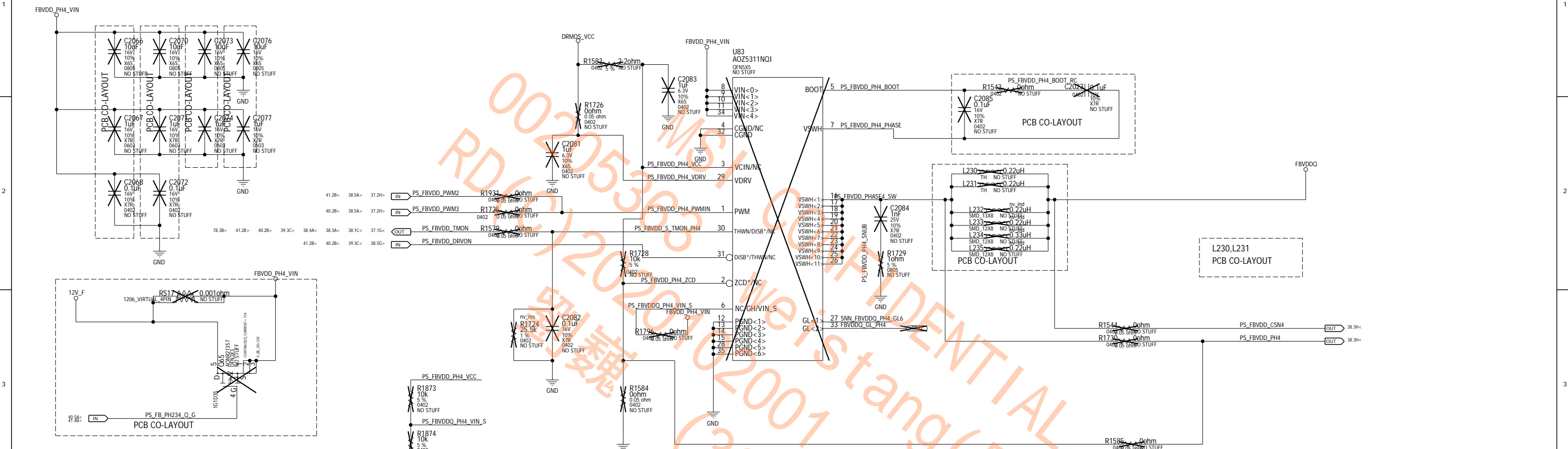


PS: FBVDD PH2

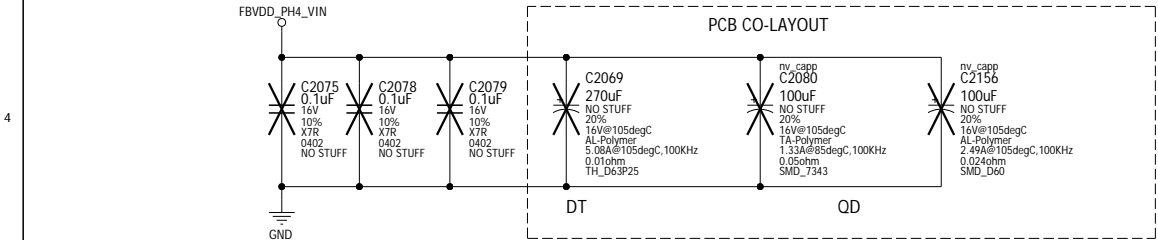


FBVDD PH2 INPUT ANTI-BACKDRIVE

PS: FBVDD PH4



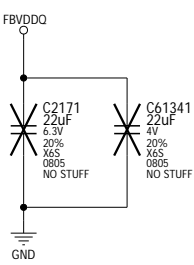
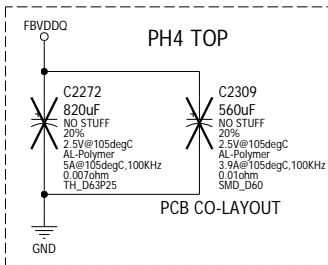
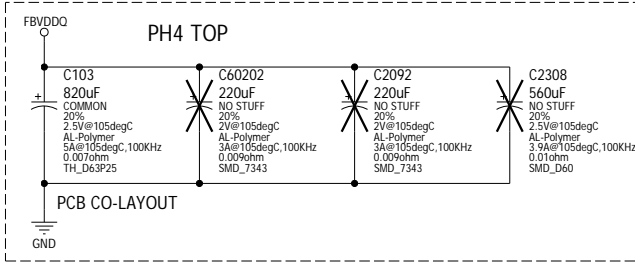
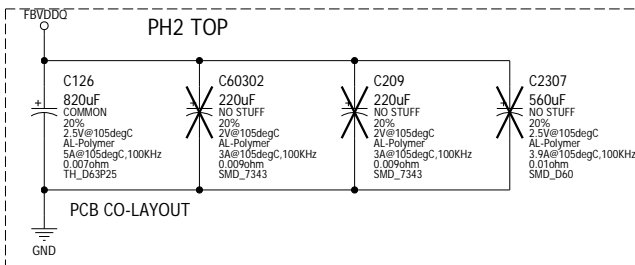
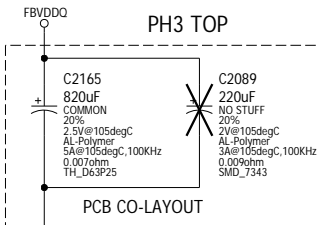
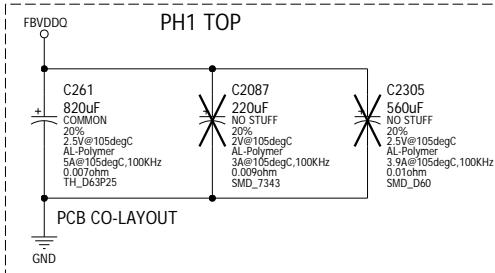
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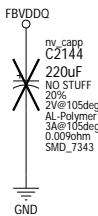
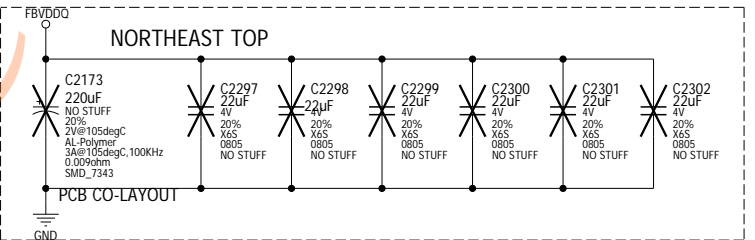
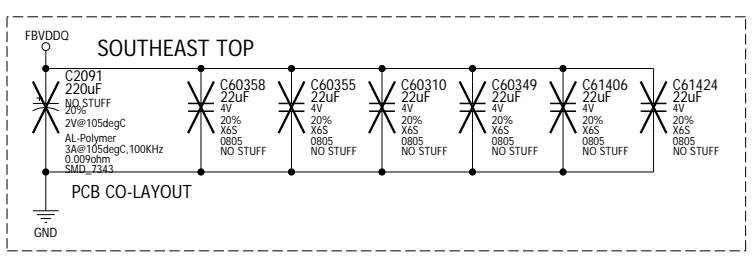
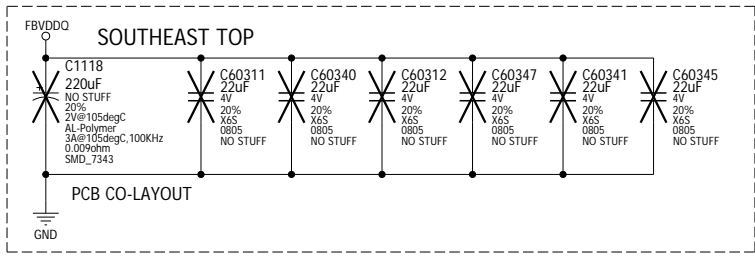
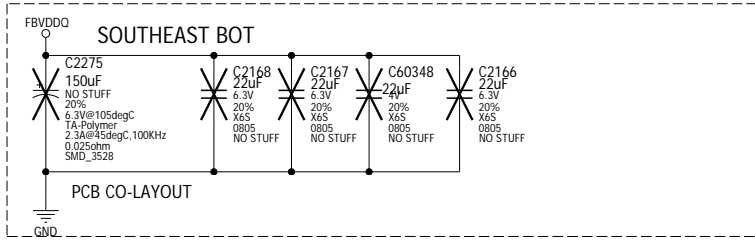
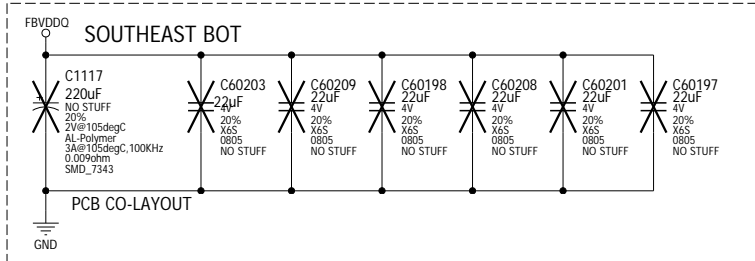
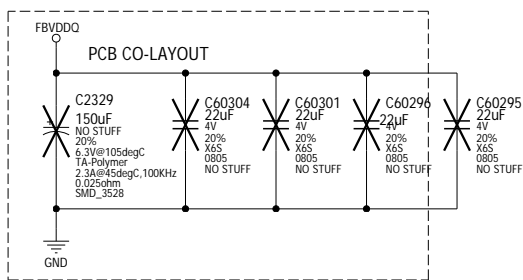
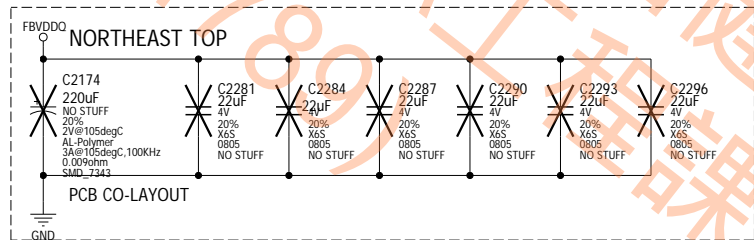
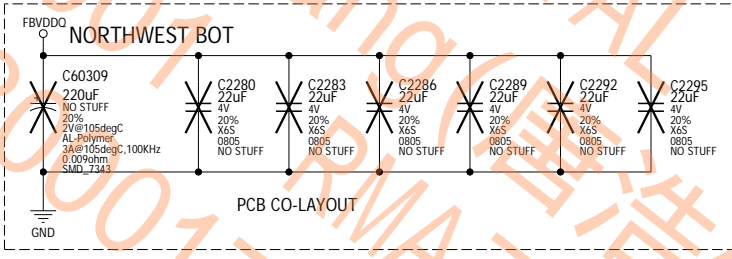
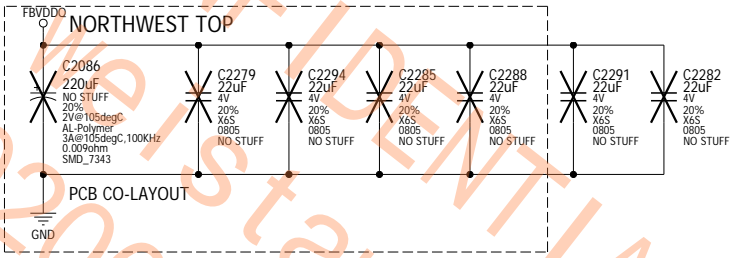
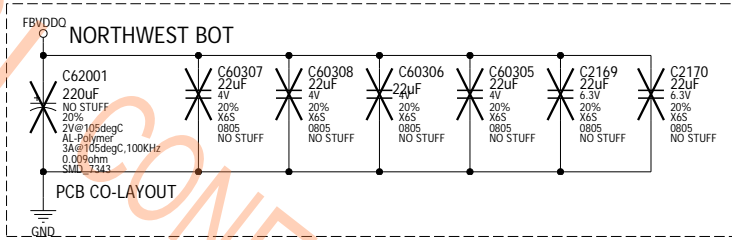
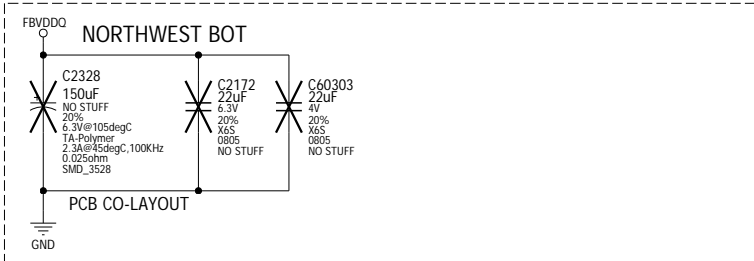
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PS: FBVDD OUTPUT CAP

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CLOSE TO FB PH3 OUTPUT STUFF



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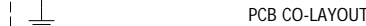
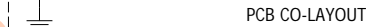
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PAGE DETAIL	PS: FBVDD_OUTPUT_CAP_NEAR_MEMORY

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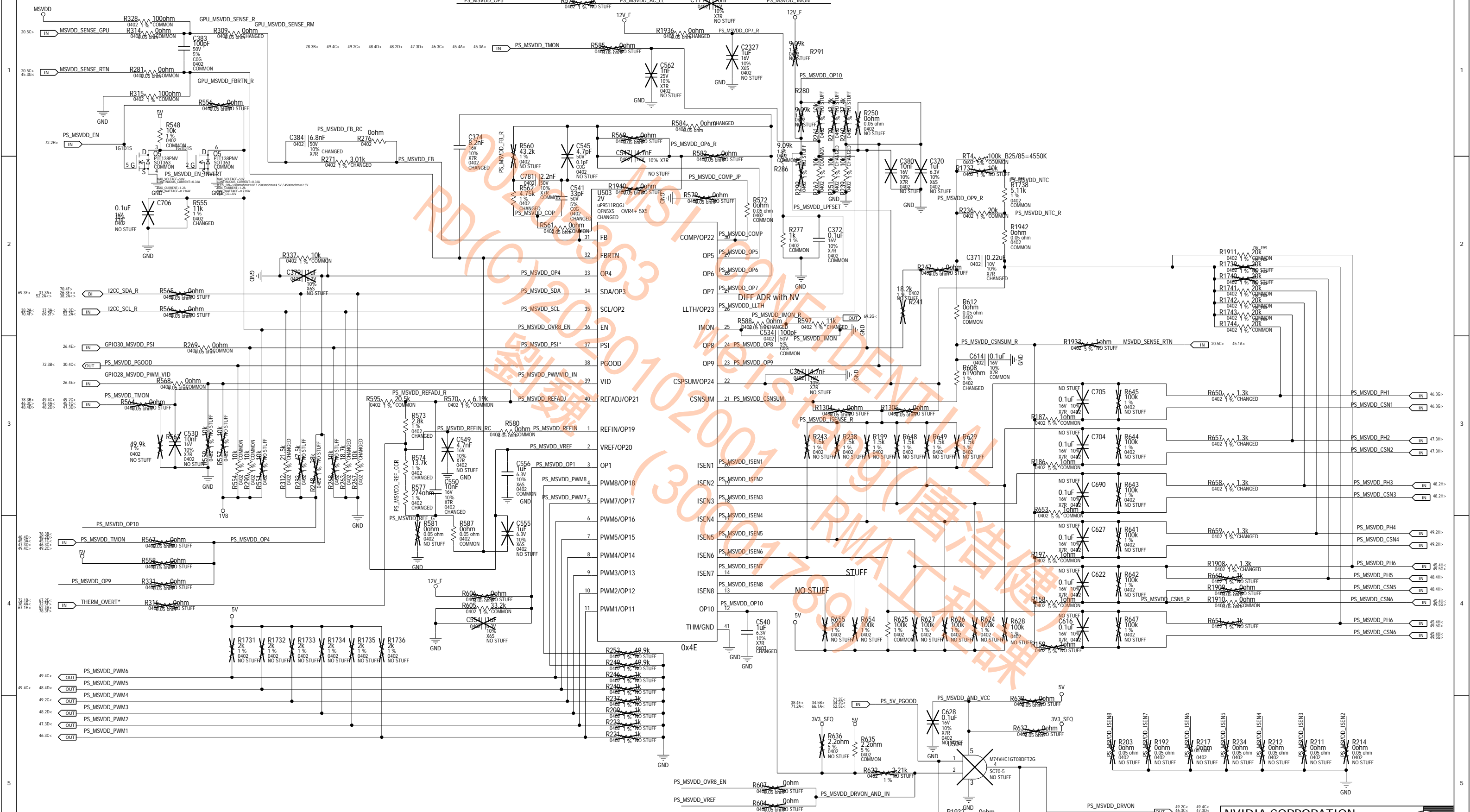
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## PS: MSVDD



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PAGE DETAIL	PS: MSVDD CONTROLLER

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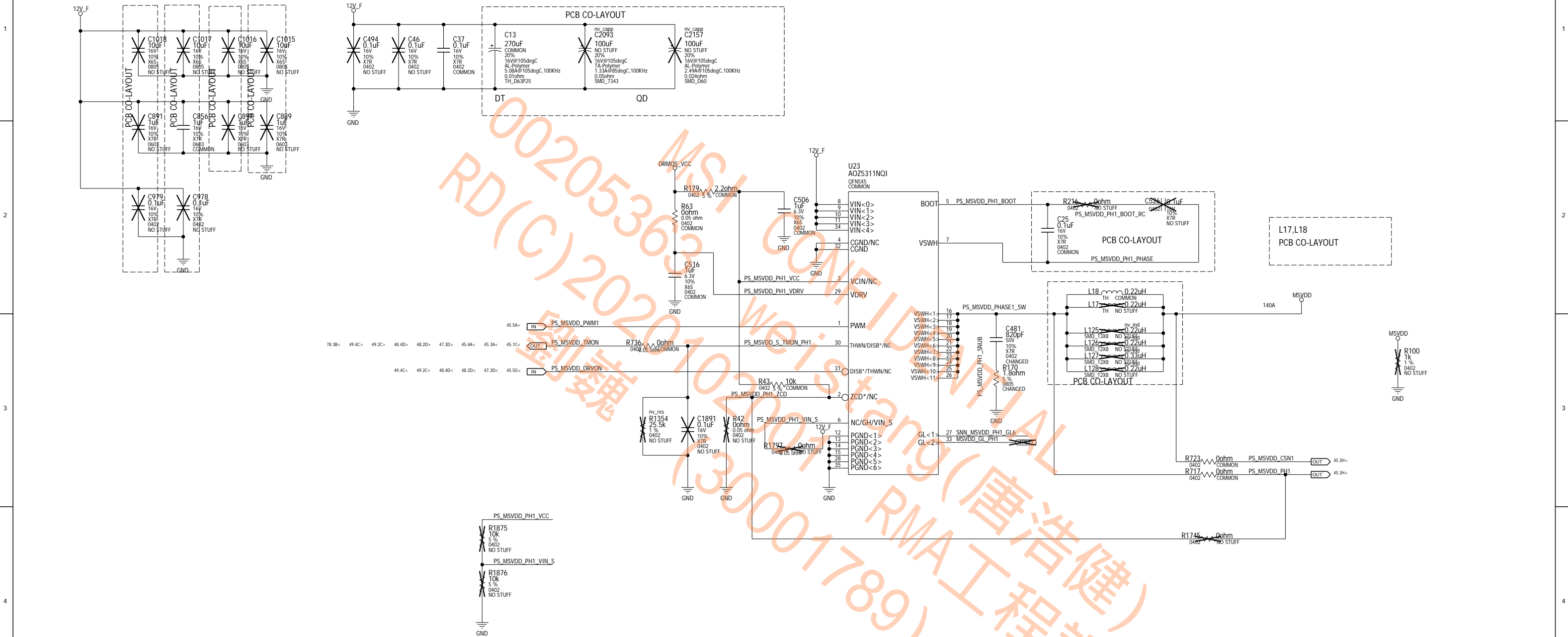
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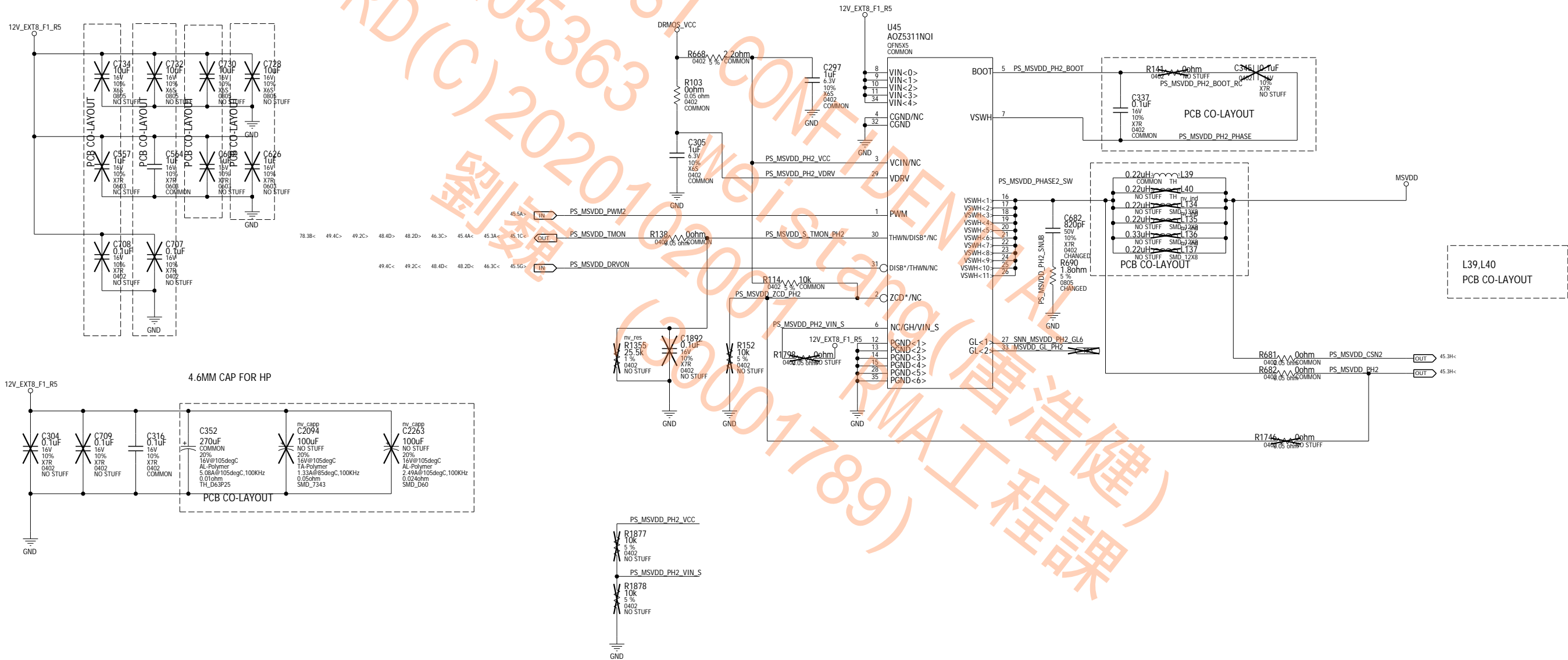
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PS: MSVDD Phase 1



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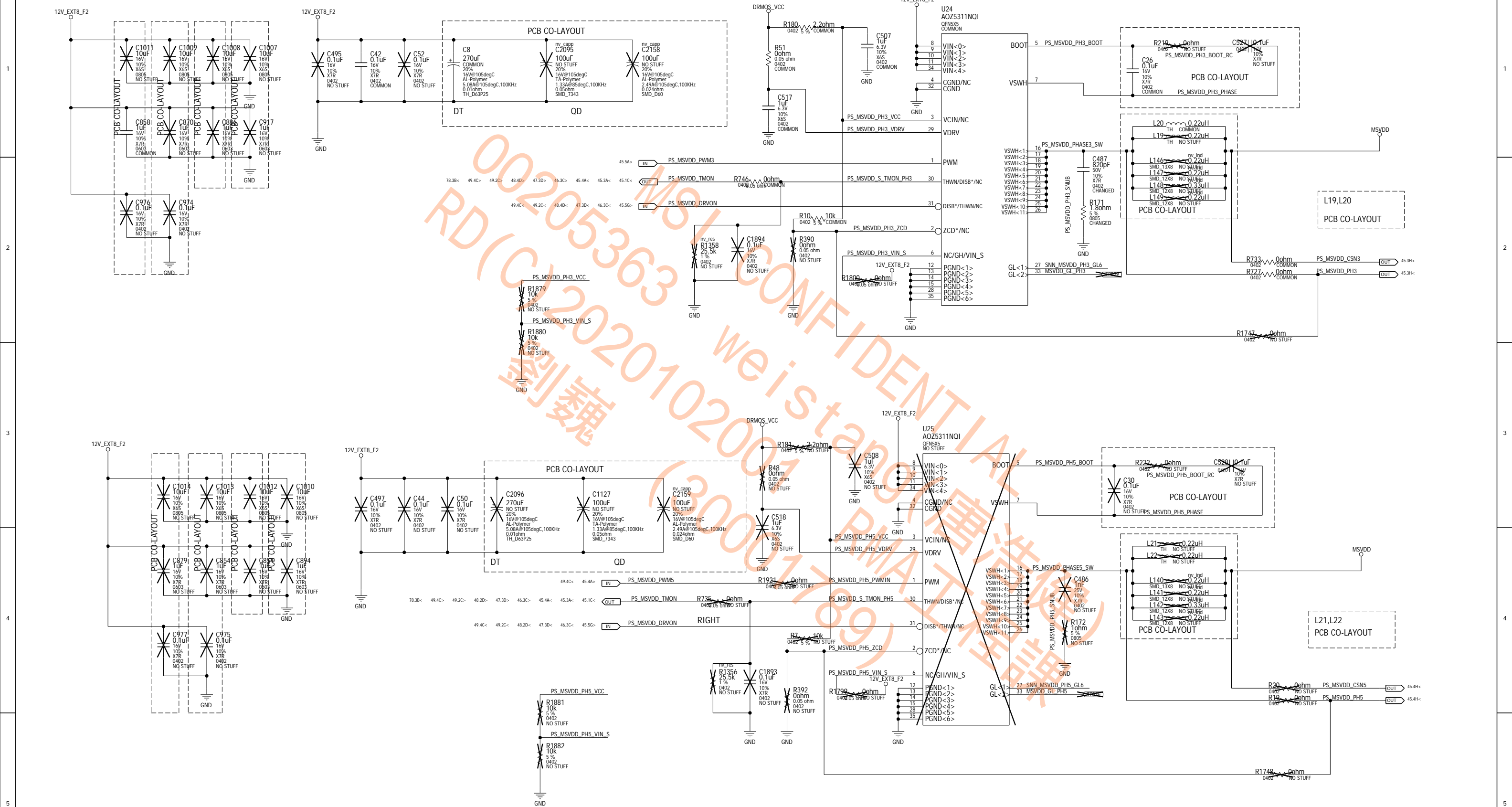
PS: MSVDD PH 2



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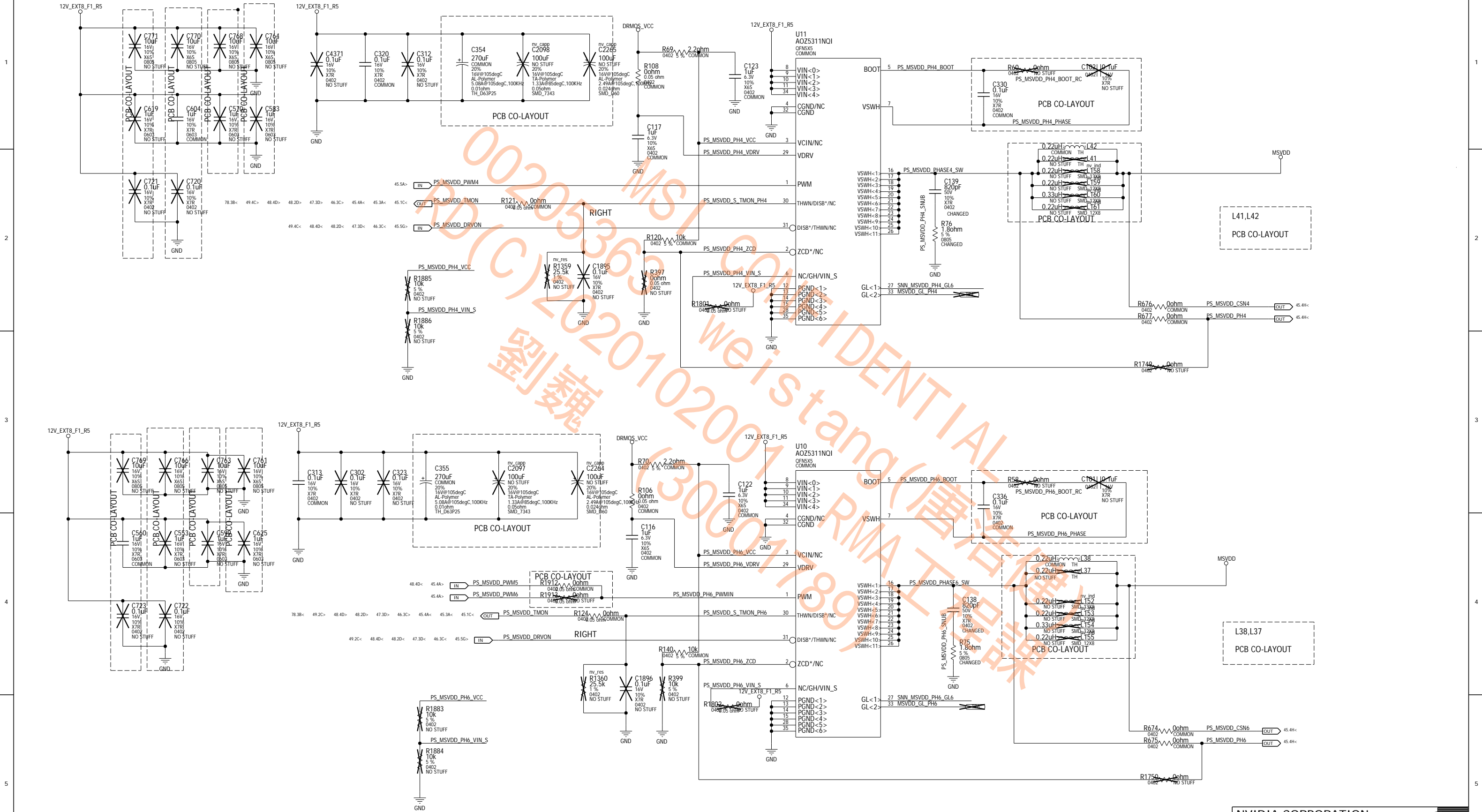


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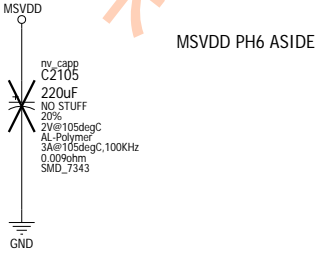
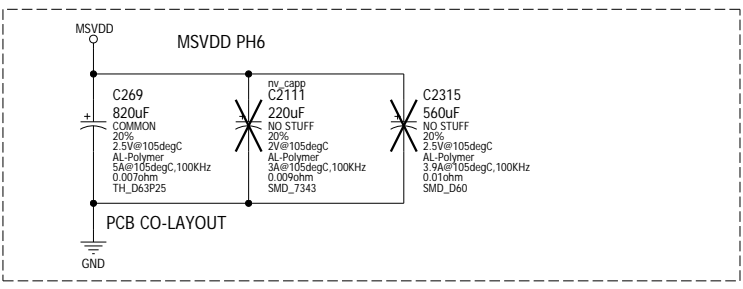
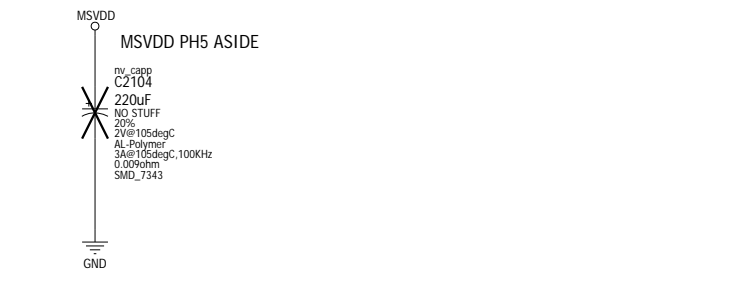
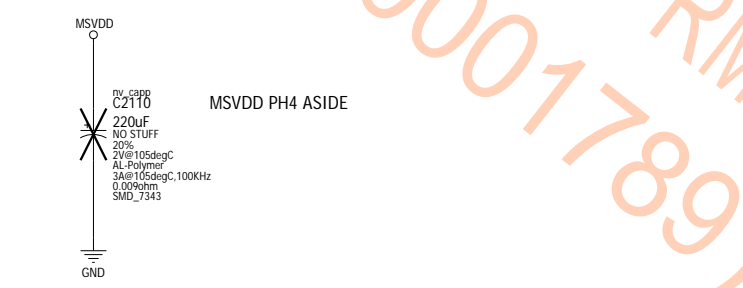
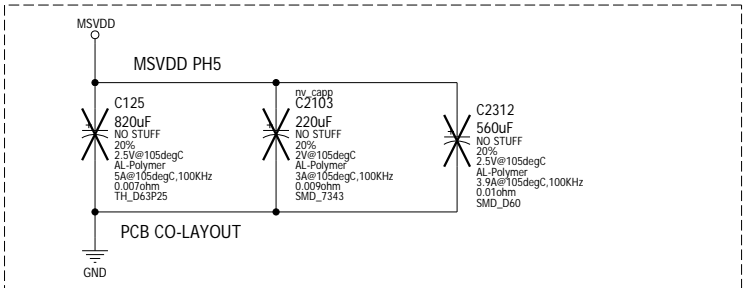
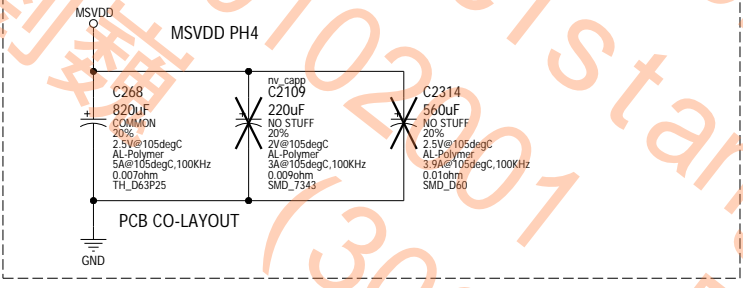
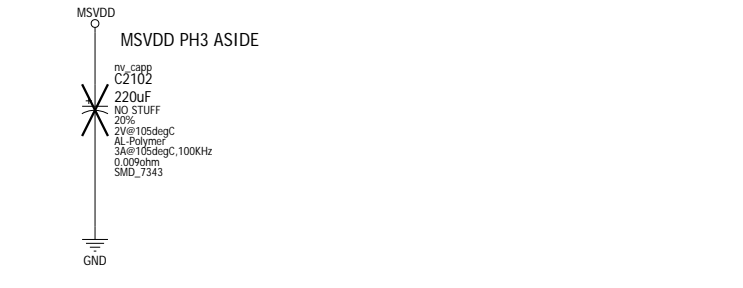
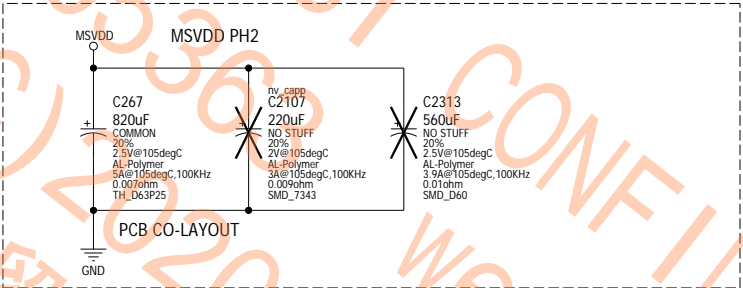
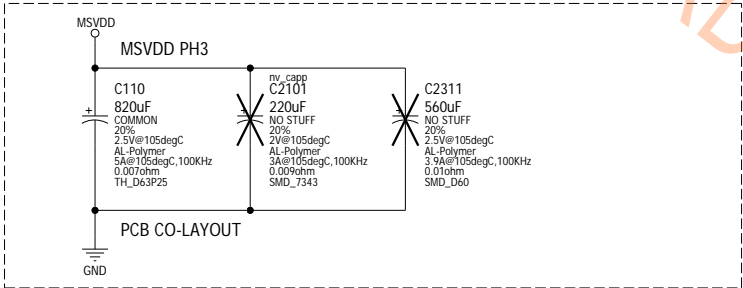
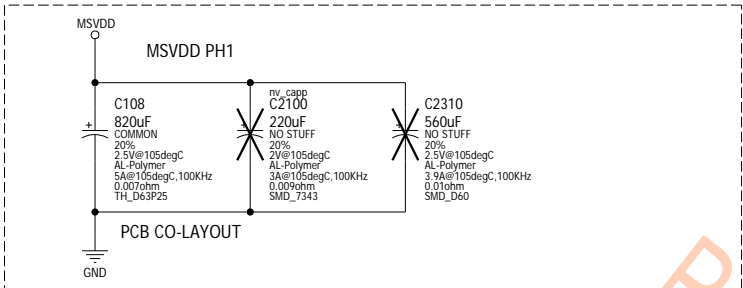
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PS: MSVDD PH 4,6



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PS:MSVDD OUTPUT CAP (TOP)



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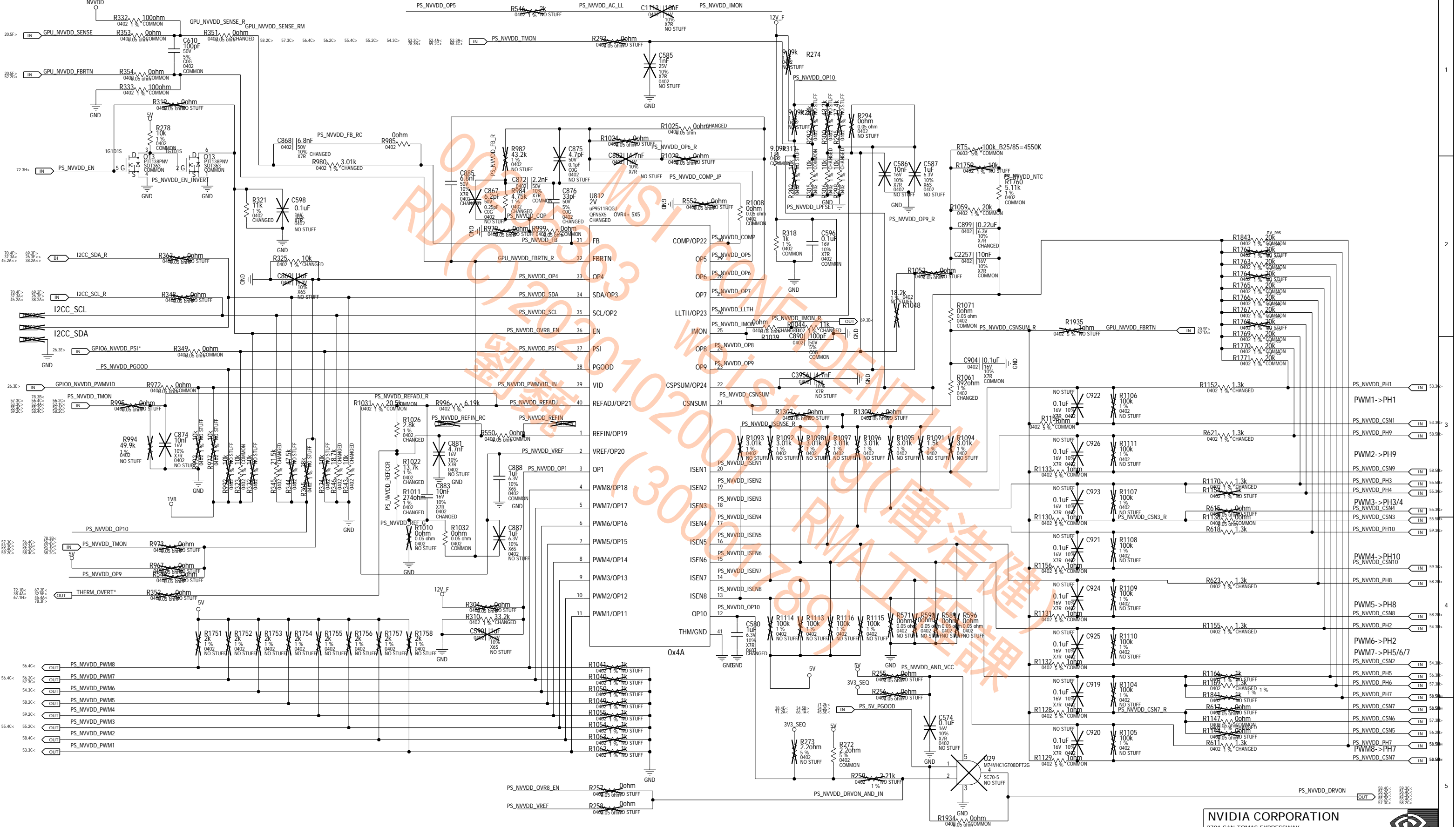
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## PS: NVVDD Controller\_OVR8



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PAGE DETAIL	PS: NVVDD Controller_OVR8

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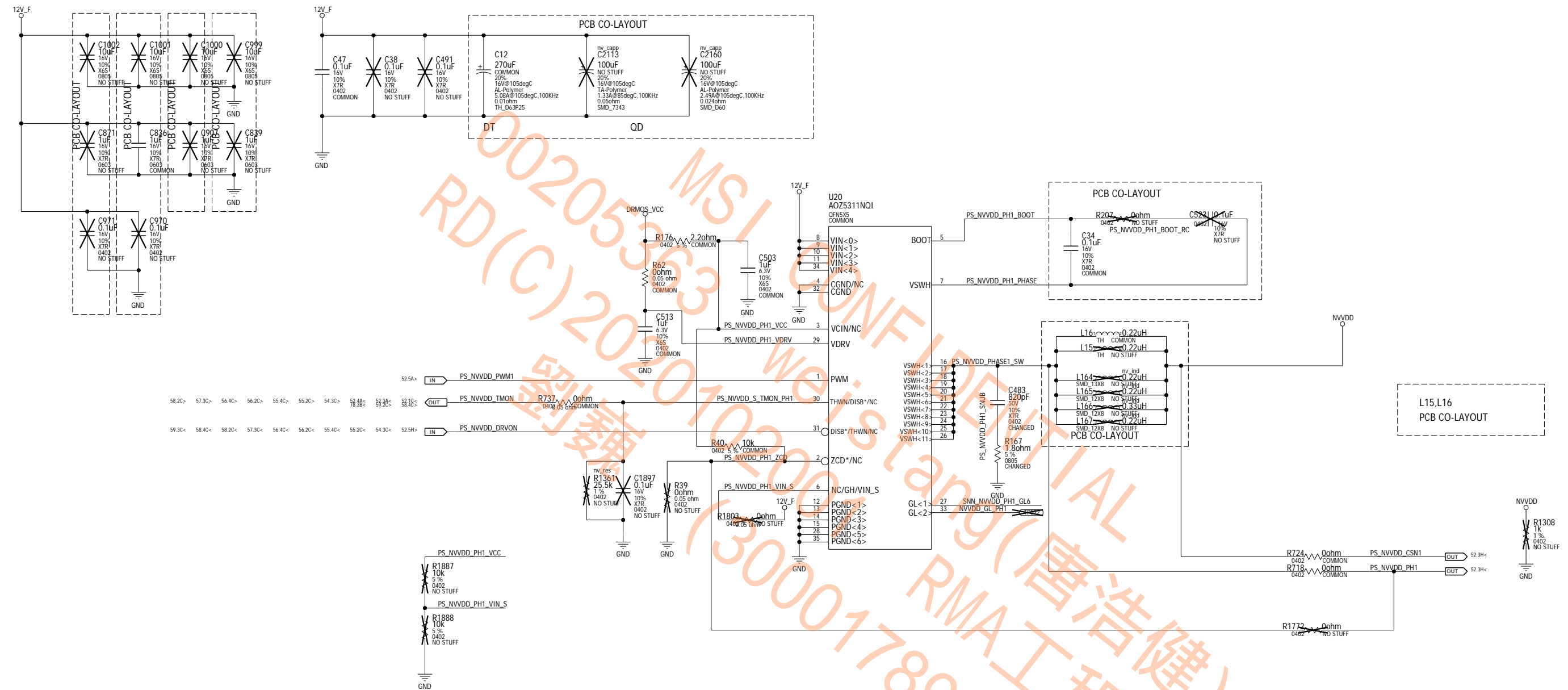
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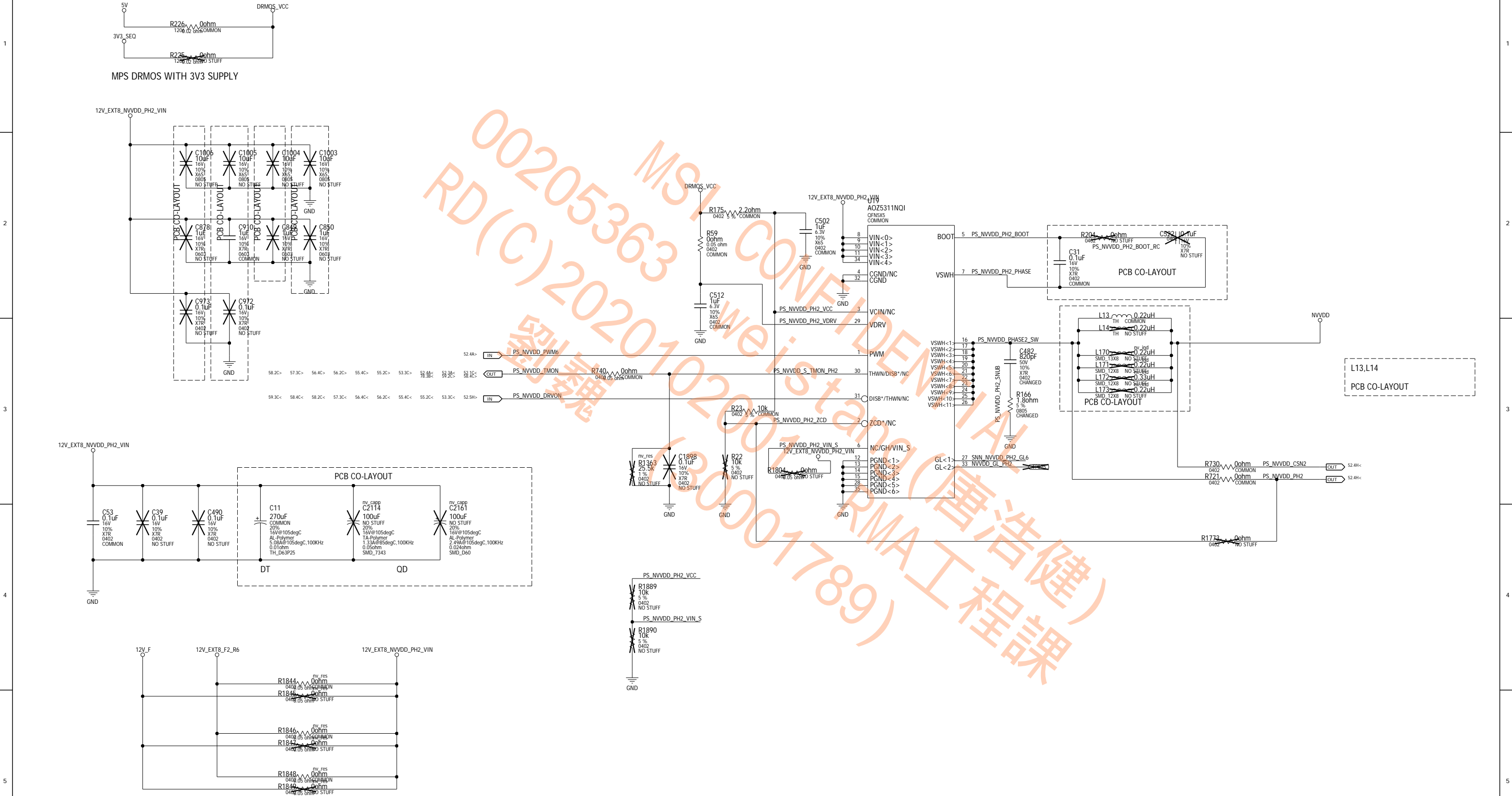
## PS: NVVDD Phase 1



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PS: NVVDD Phase 2



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PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)

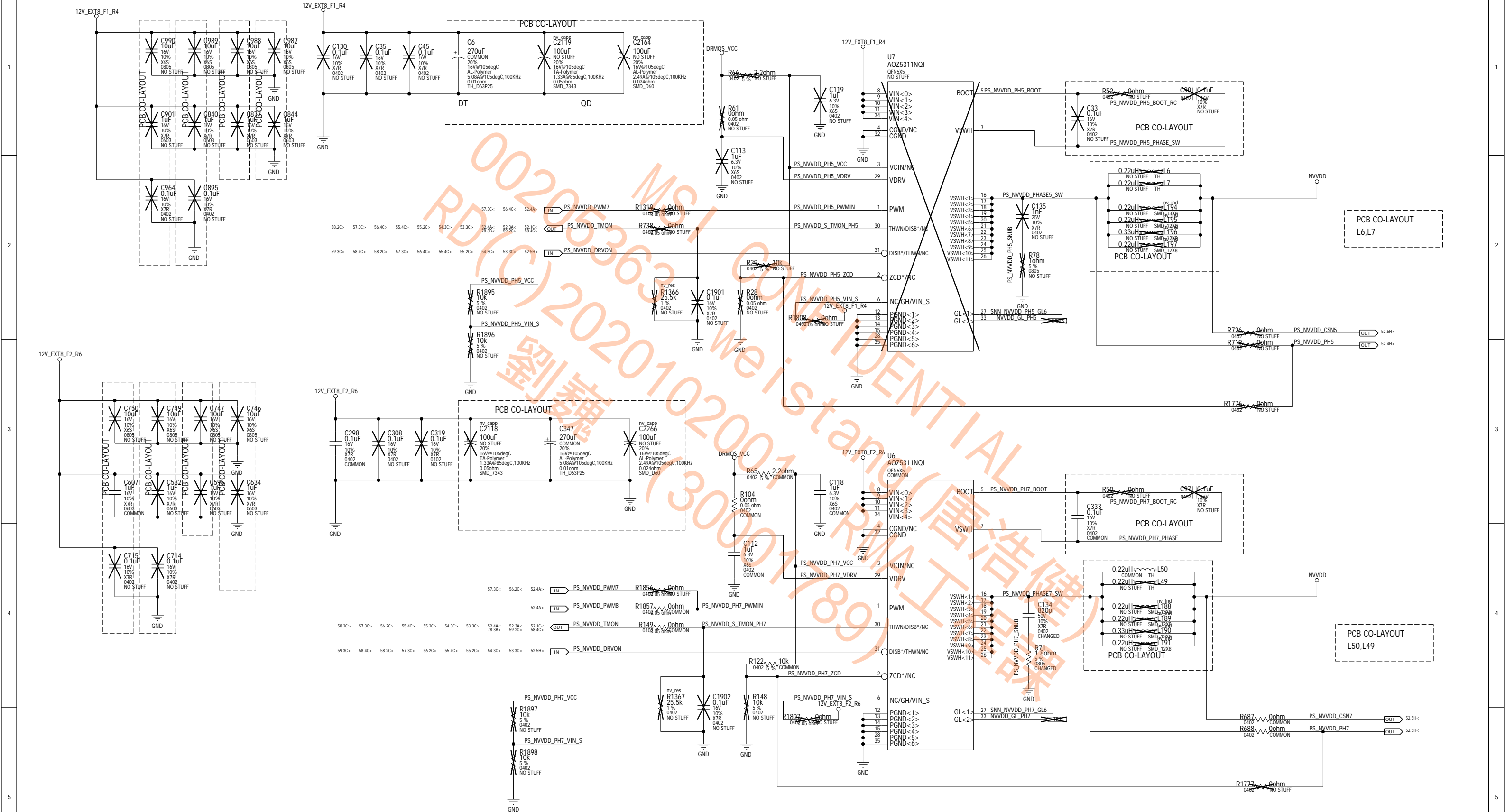
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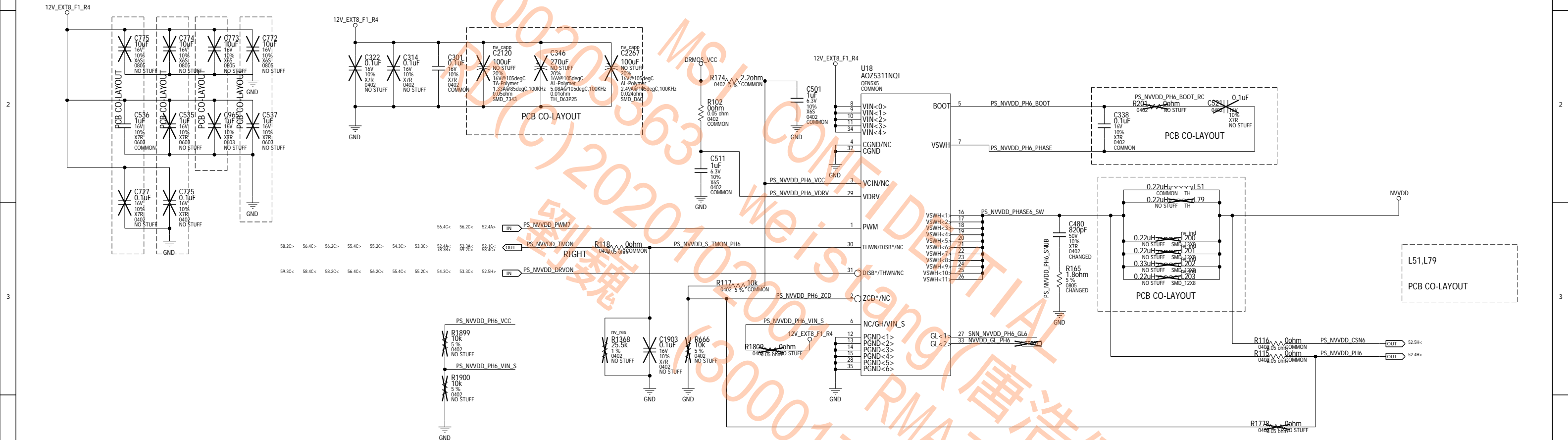
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PS: NVVDD PH 5(PWM2), PH7(PWM3)

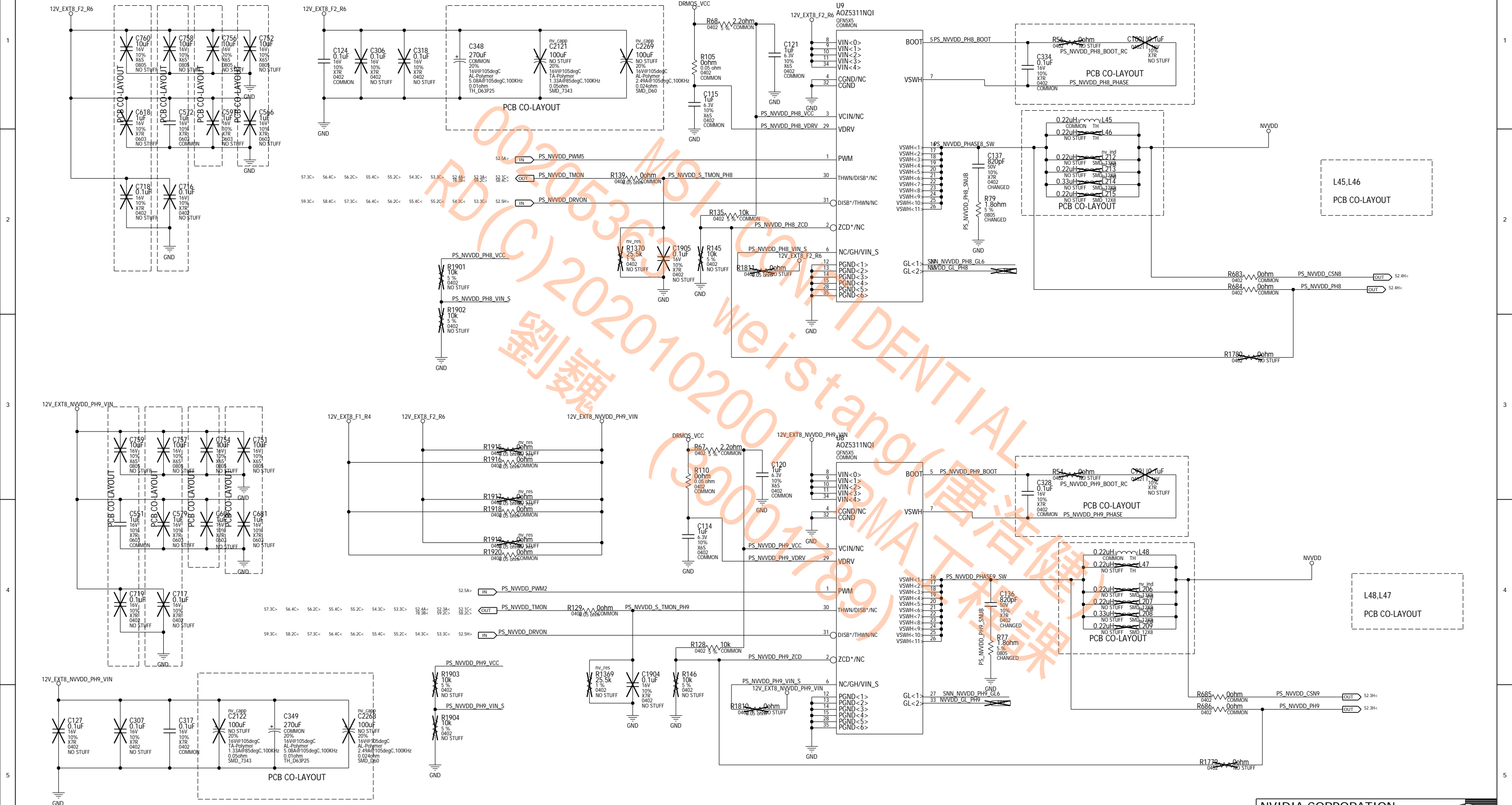


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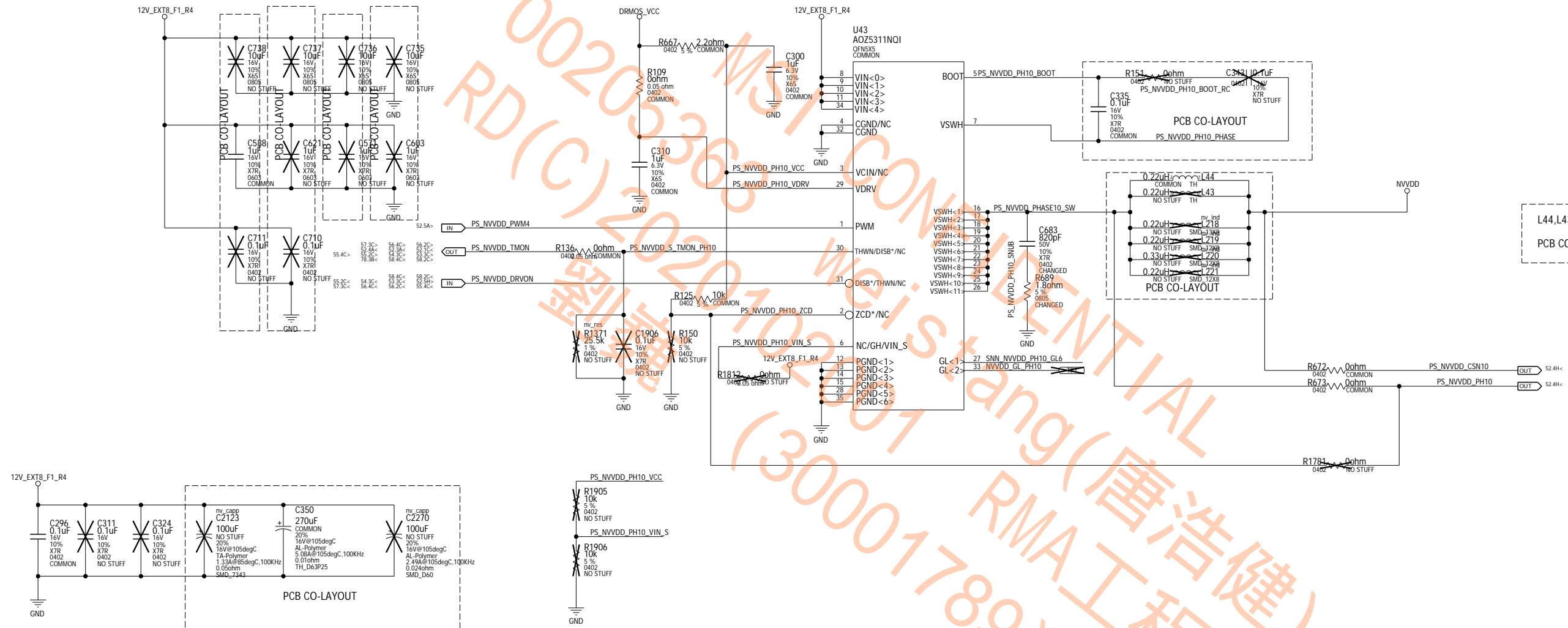


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PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



PS: NVVDD Phase 10 (PWM8)



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PCB CO-LAYOUT  
C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT  
C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C256, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005

C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96  
PCB CO-LAYOUT

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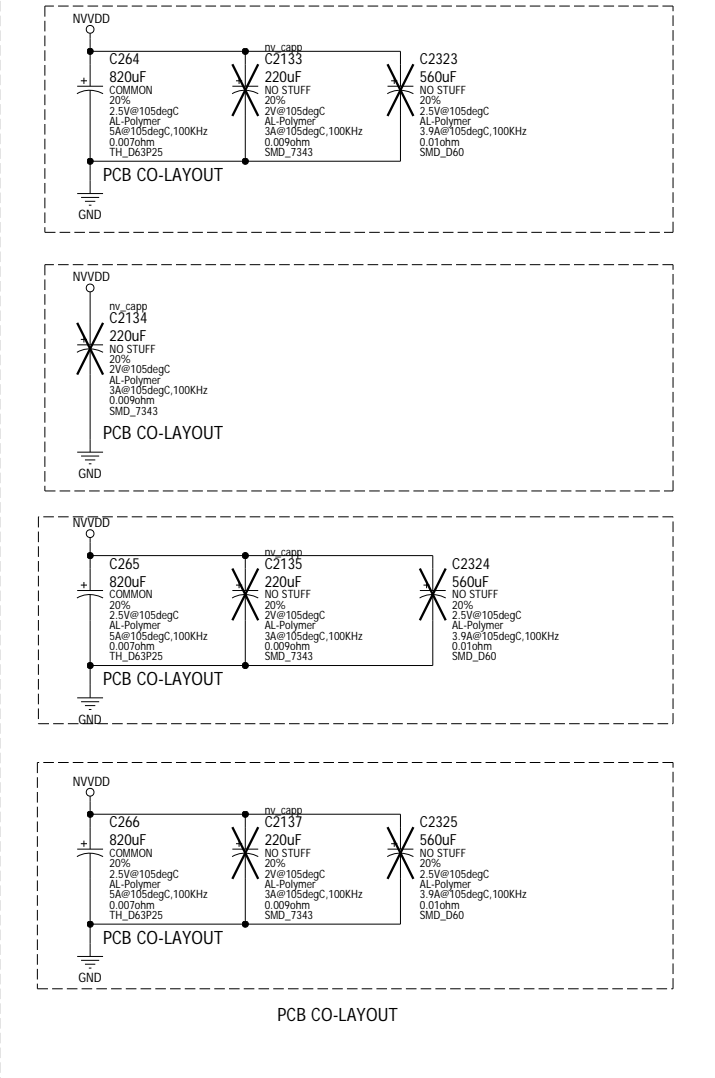
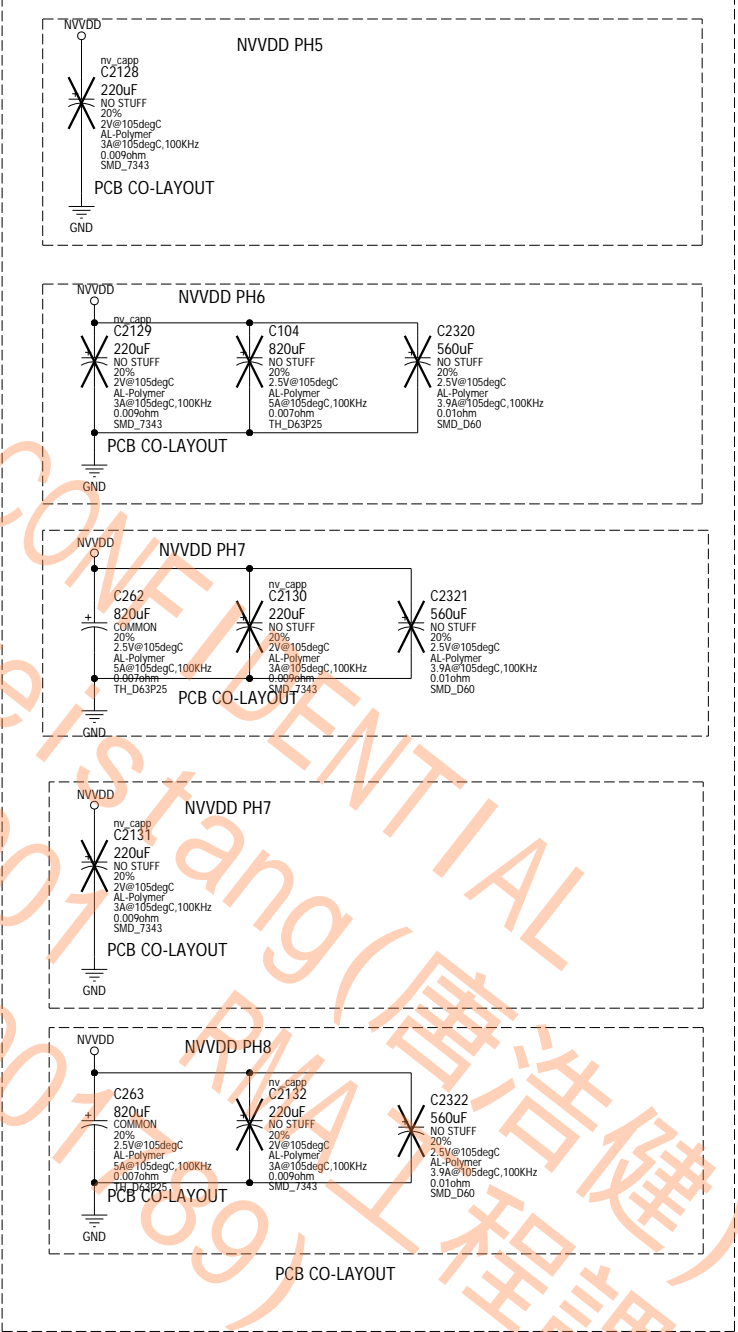
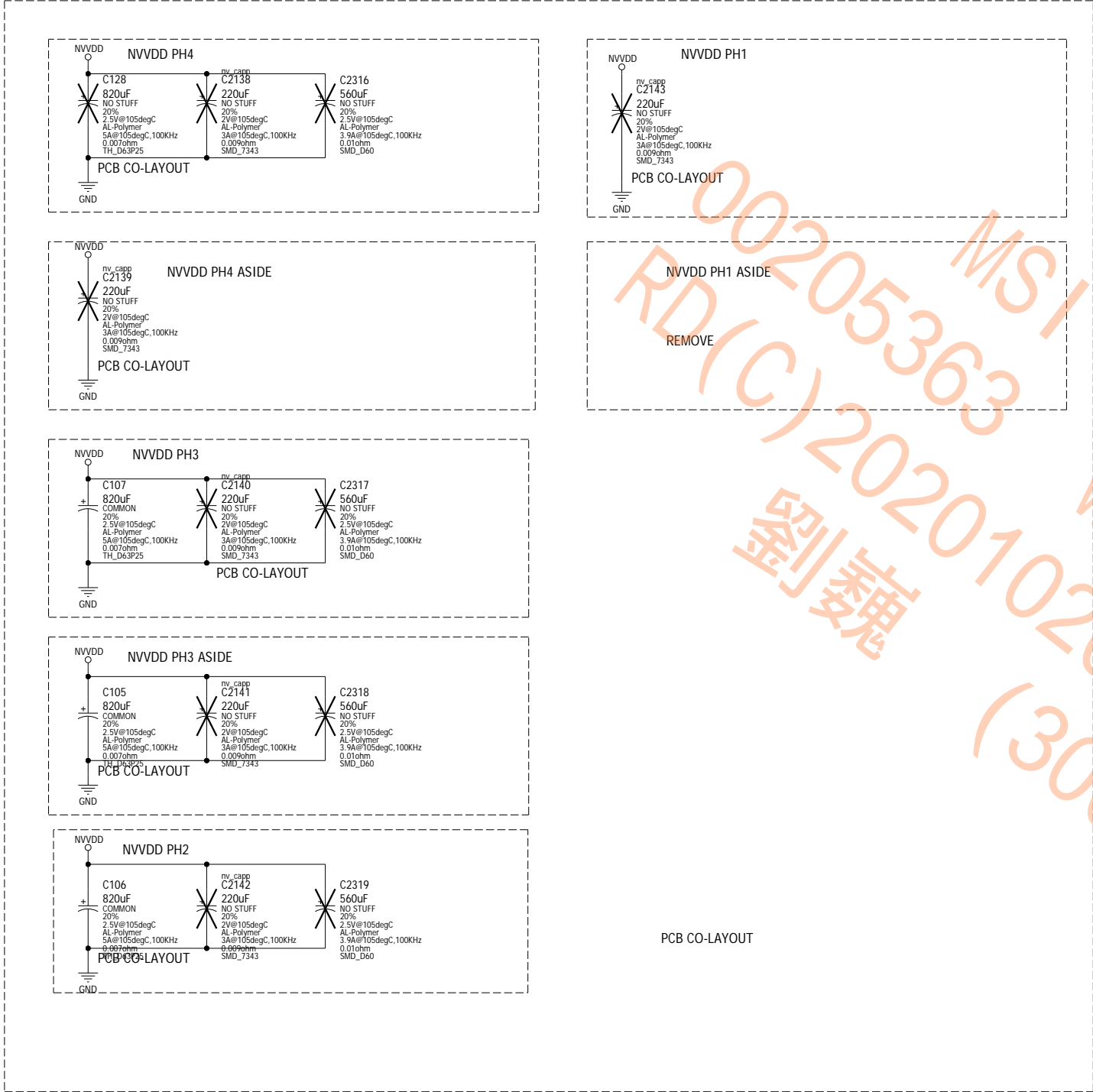
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PS: NVVDD OUTPUT CAP(TOP)



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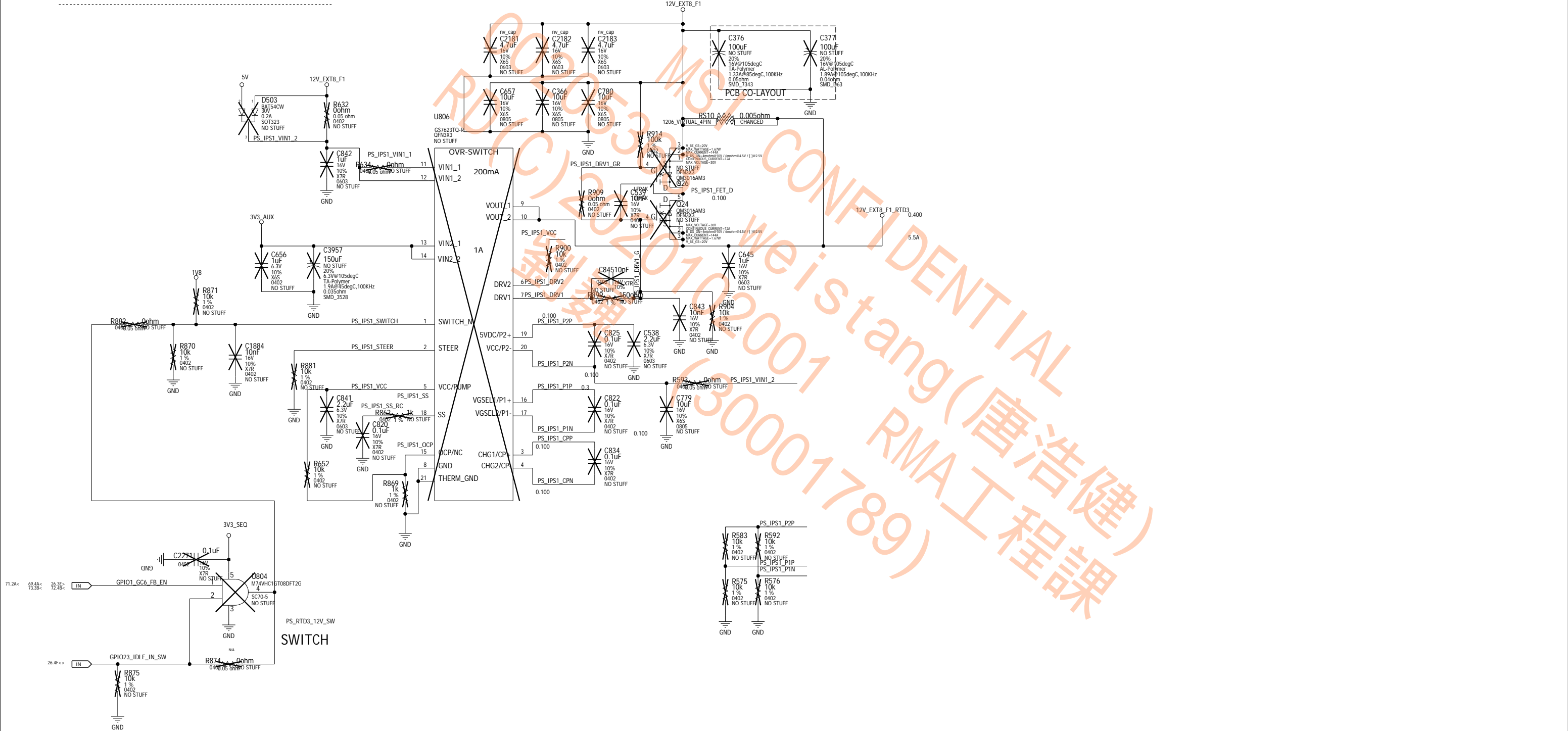
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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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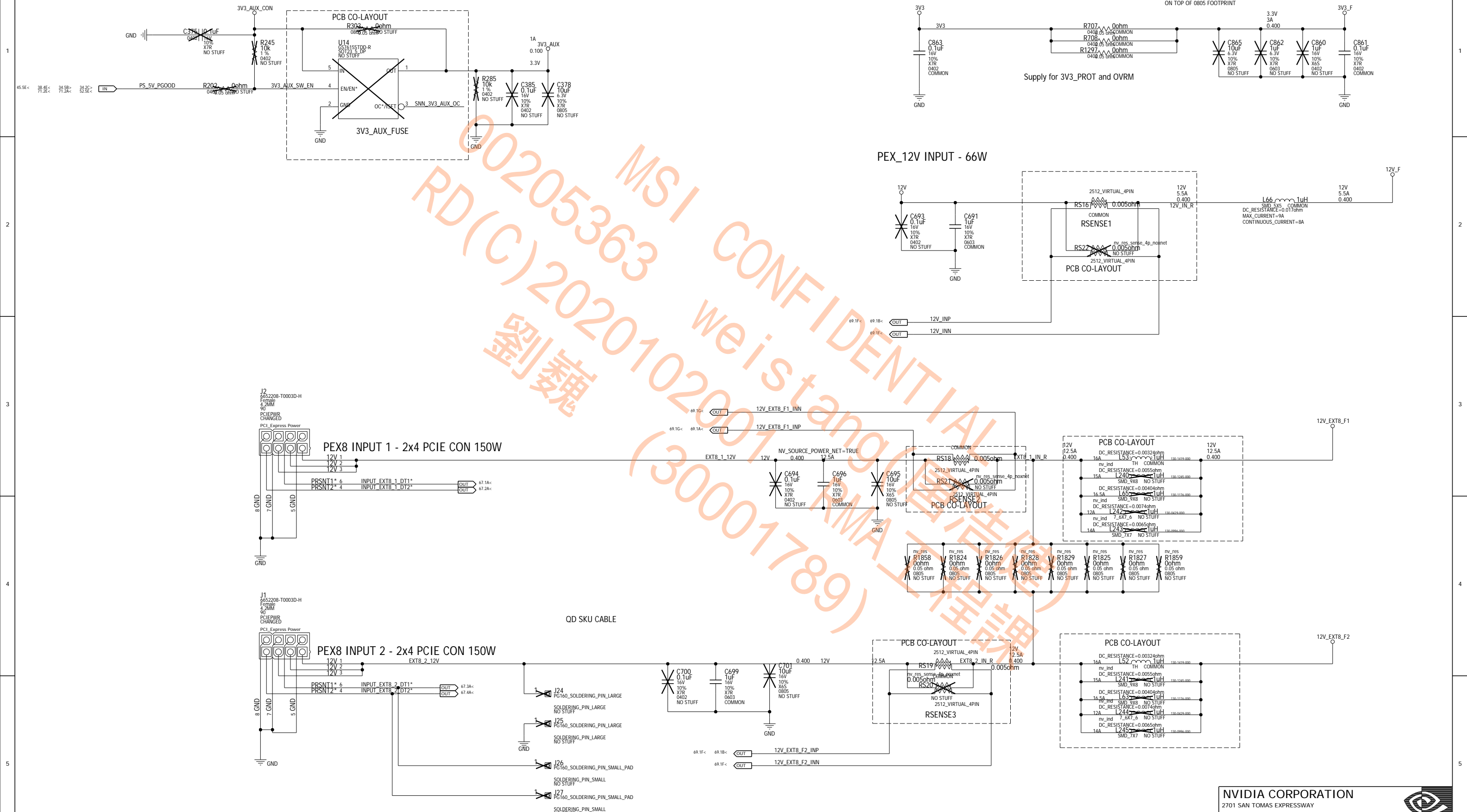
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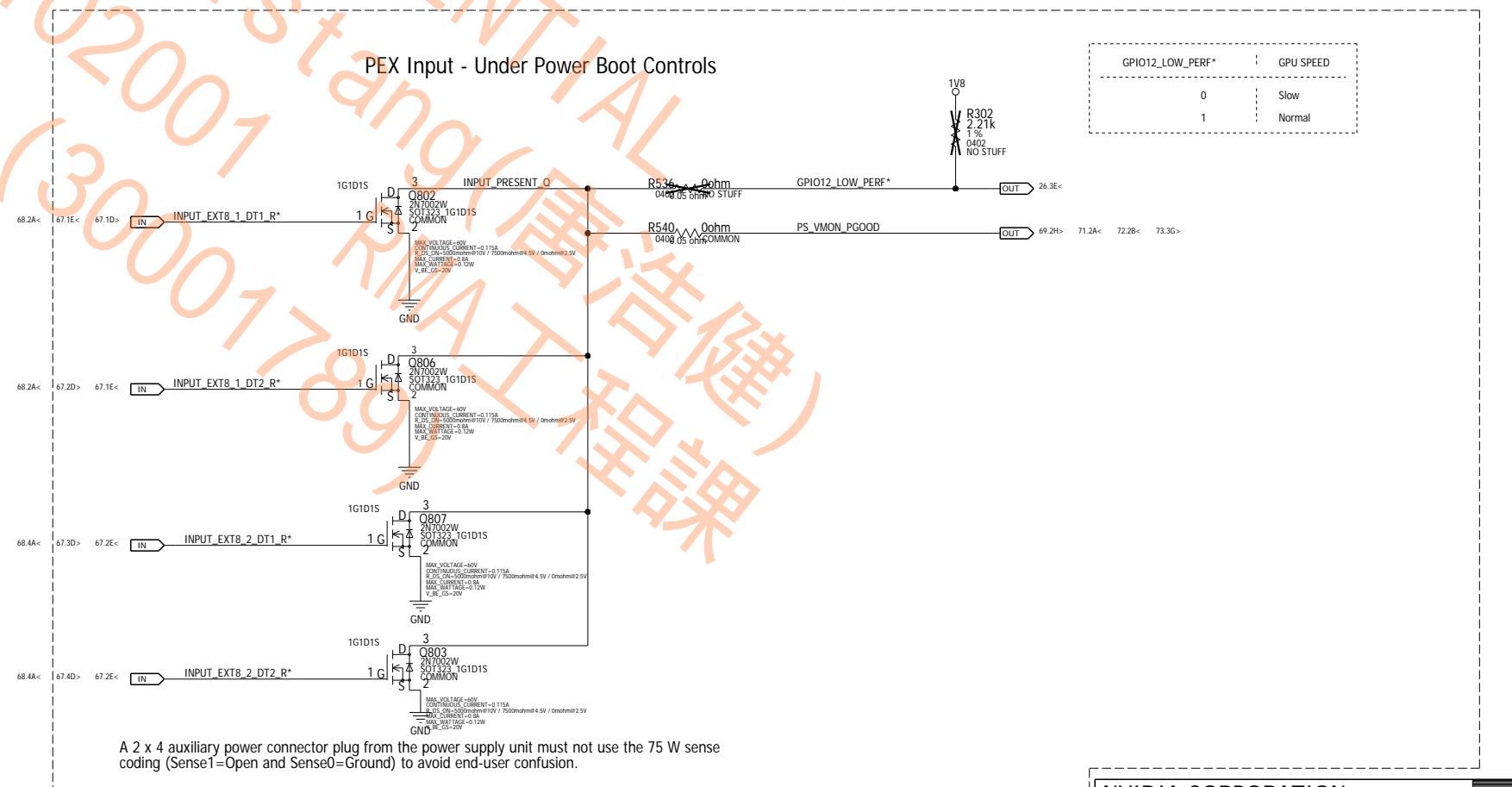
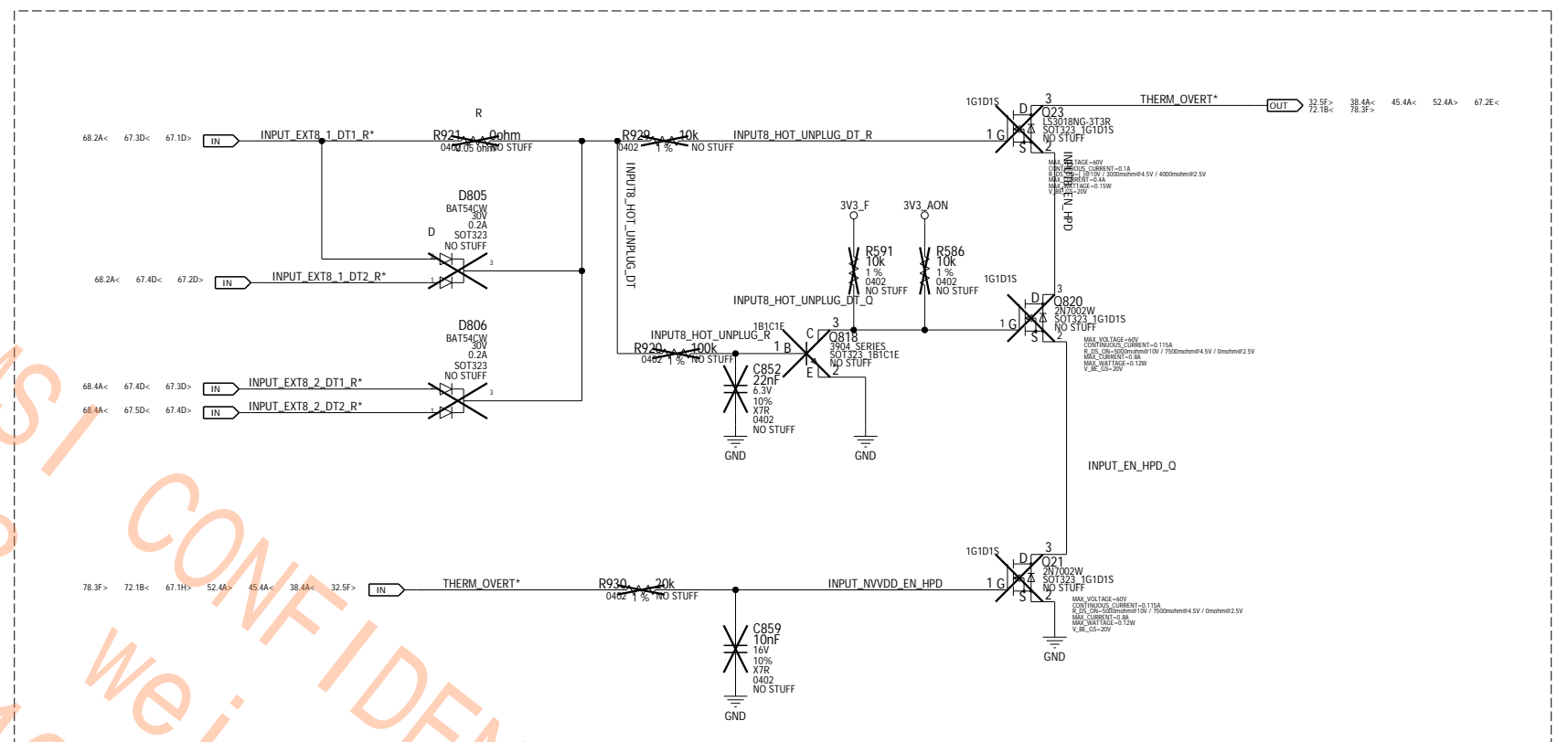
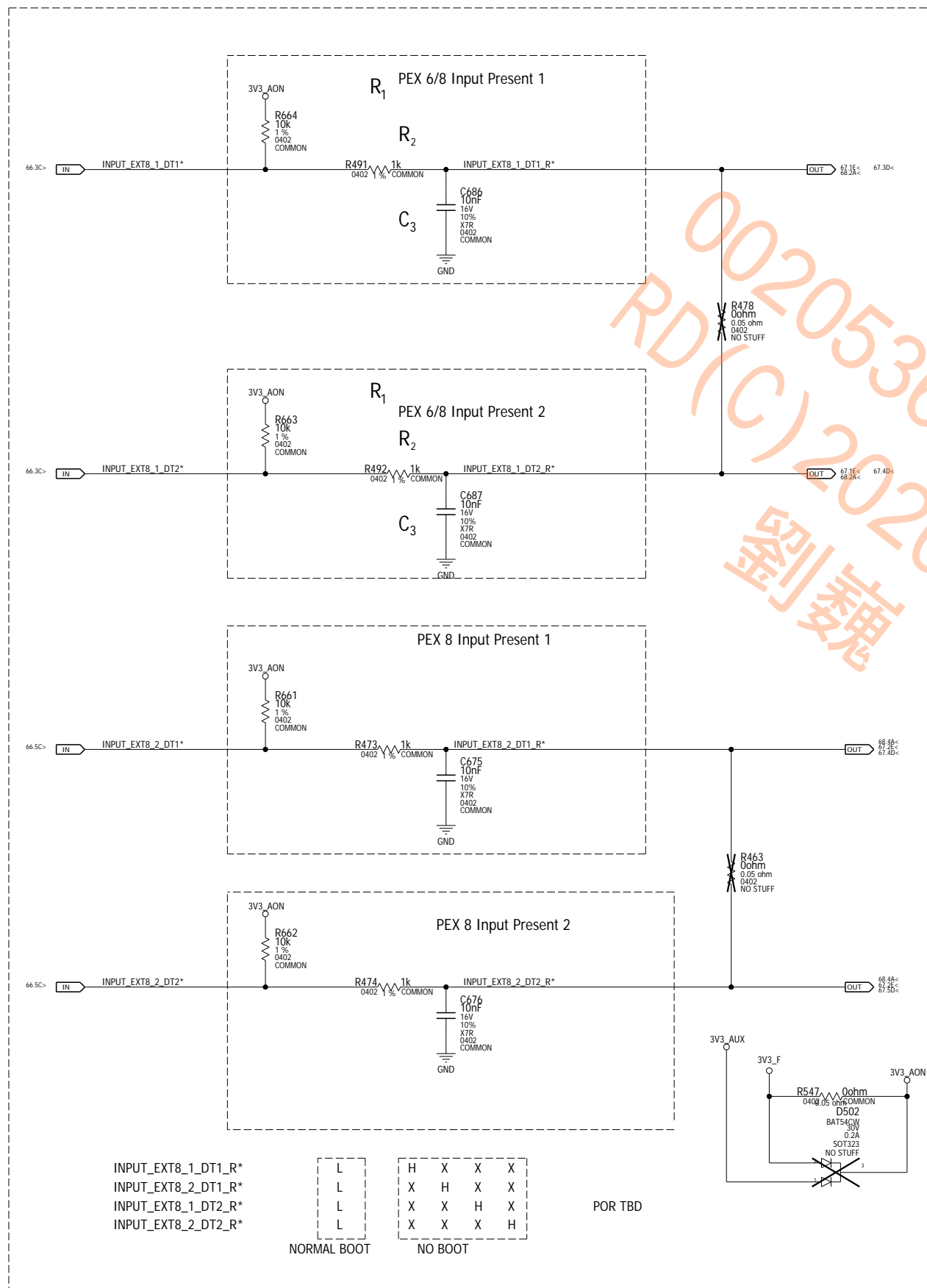
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PS: Inputs, Filtering, and Monitoring



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## PS: 12V Current Steering &amp; Hot Unplug Detect



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

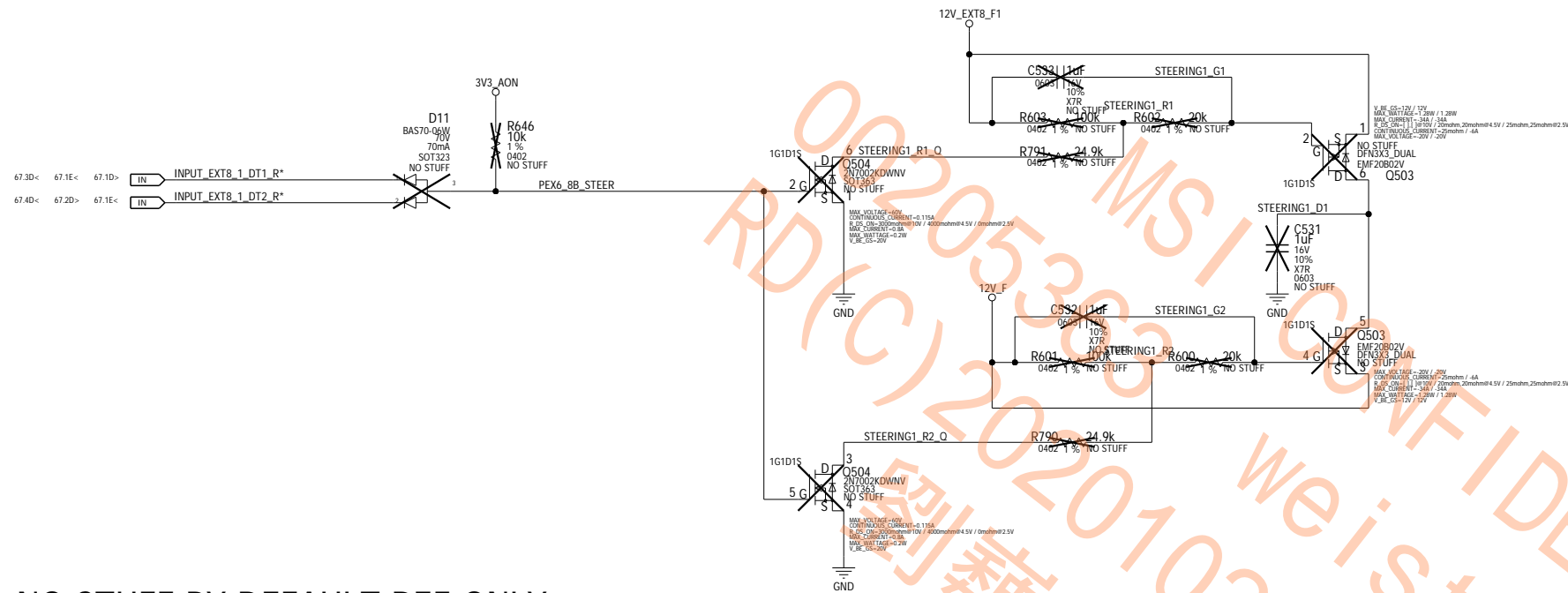
A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.



## PS: Discrete Steering

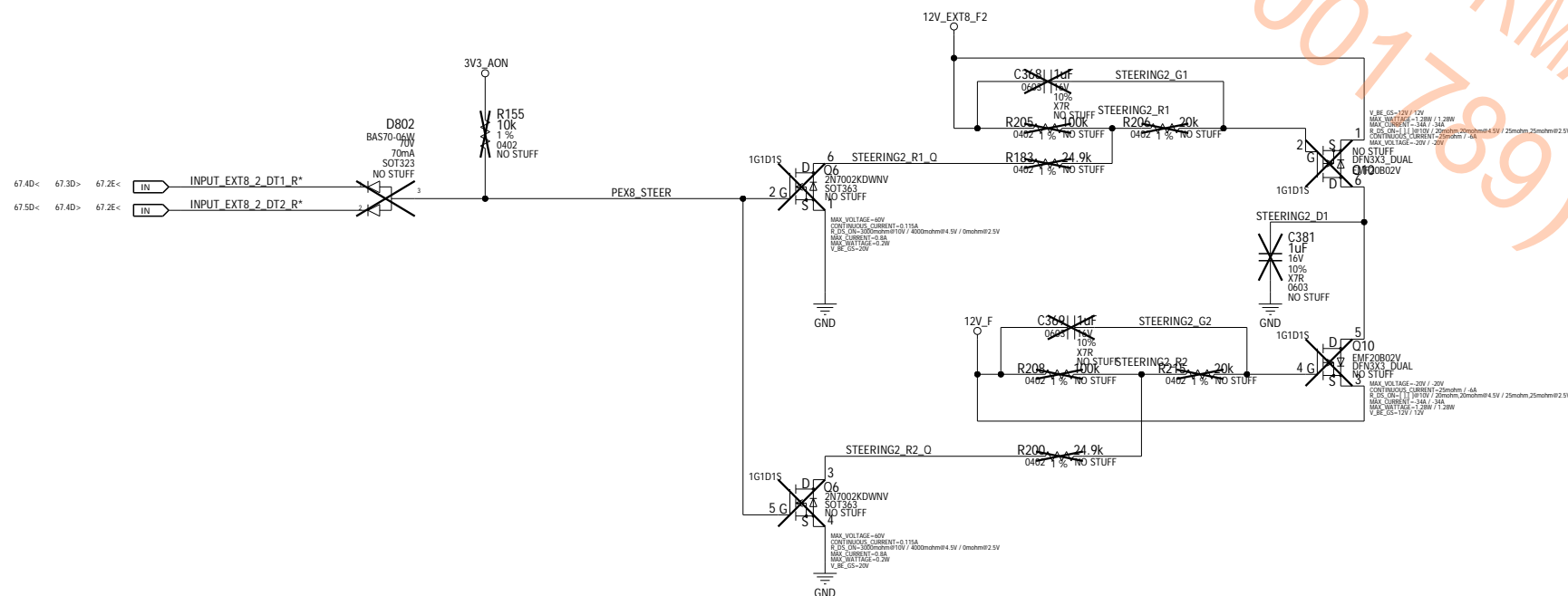
## 12V CURRENT STEERING (UNDER POWER BOOT):

## PEX12V AND 12V\_EXT8\_F1




NO STUFF BY DEFAULT REF ONLY

## PEX12V AND 12V\_EXT8\_F2

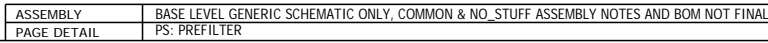


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PAGE DETAIL	PS: Discrete Power Steering

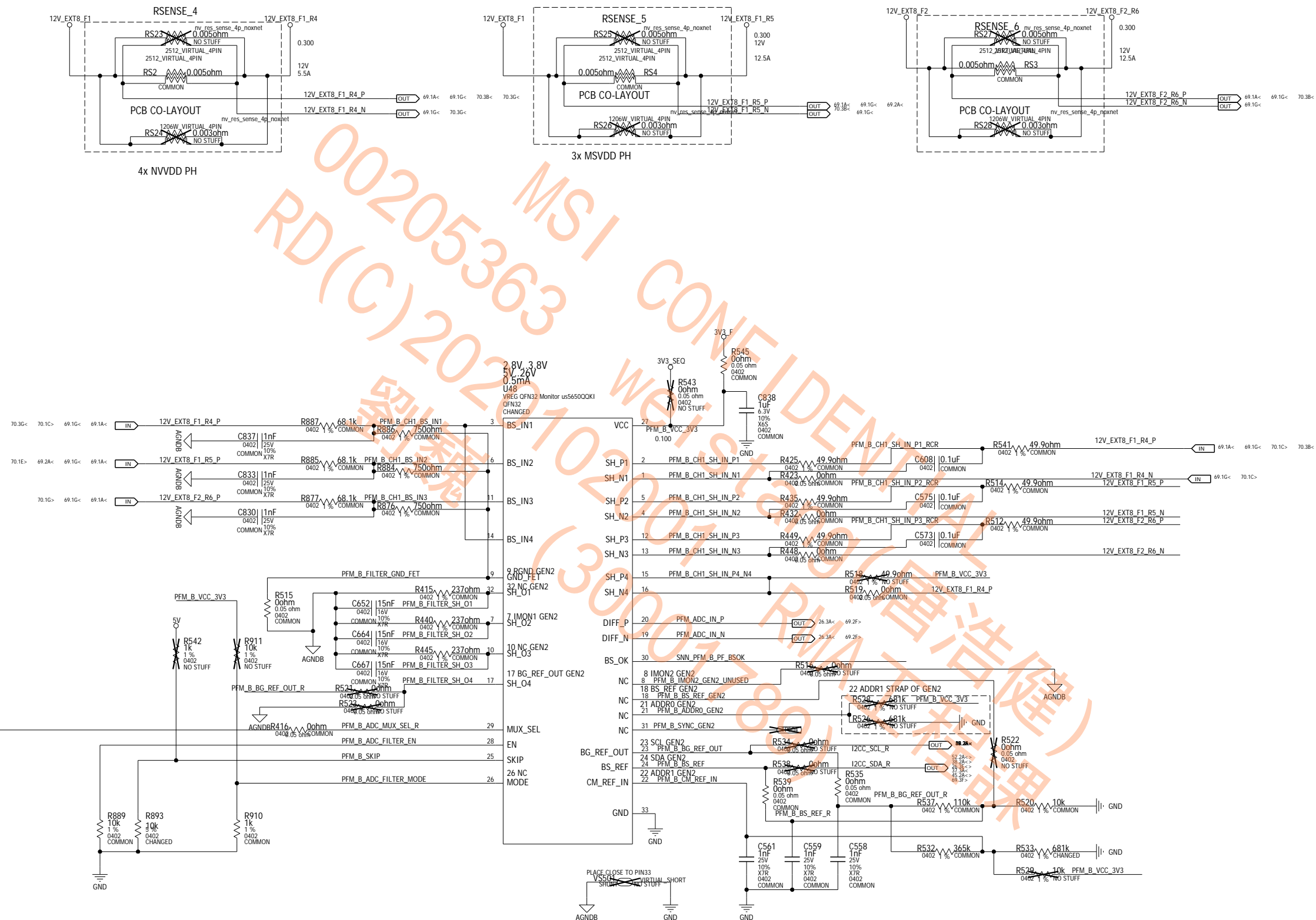
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## Route the trace to PEX Golden Finger




PS: Pre-Filter B

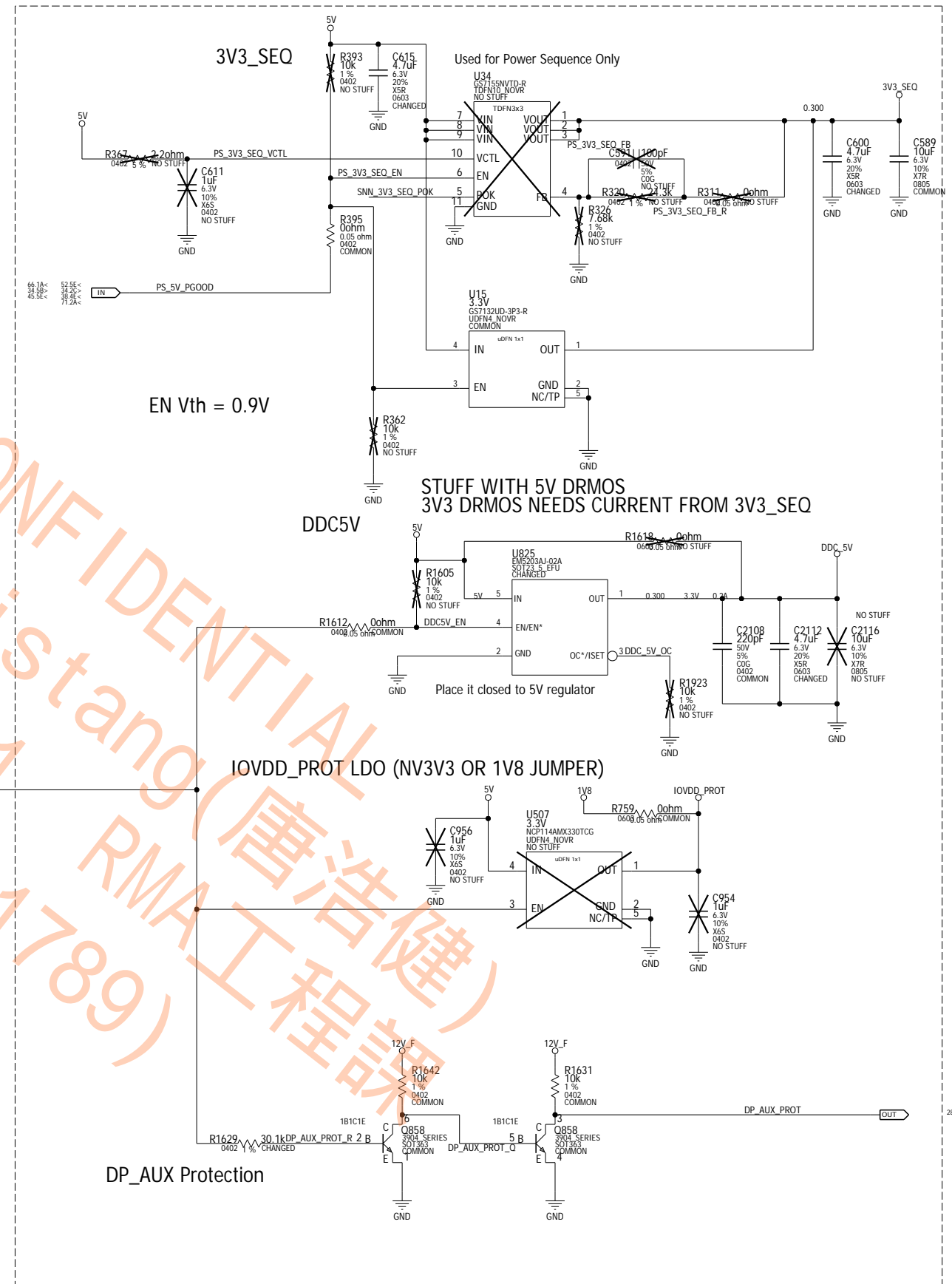
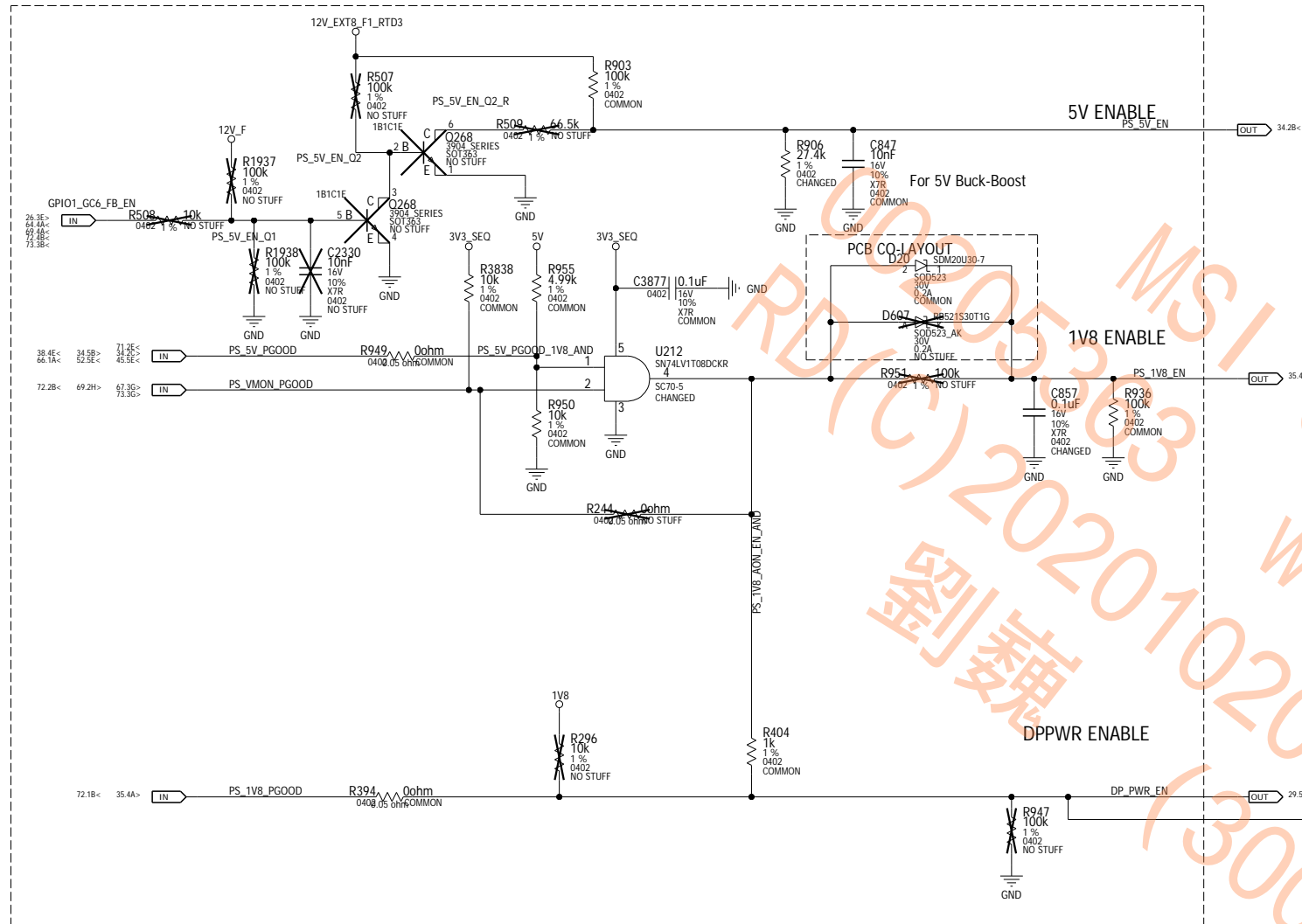


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SEQUENCE:5V,1V8,3V3\_SEQ ENABLE



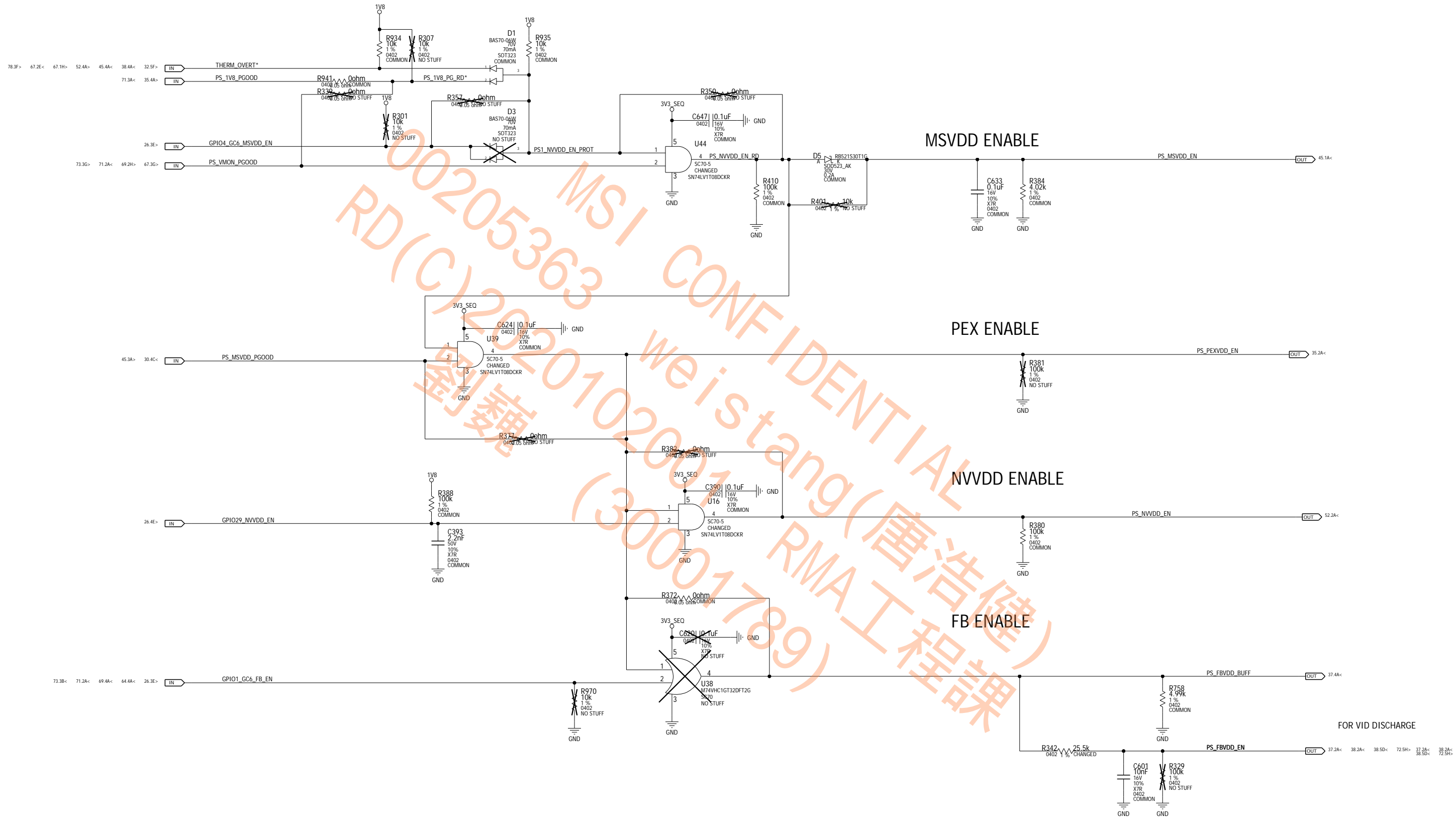
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PAGE DETAIL	Sequence: 5V, 1V8, 3V3_SEQ

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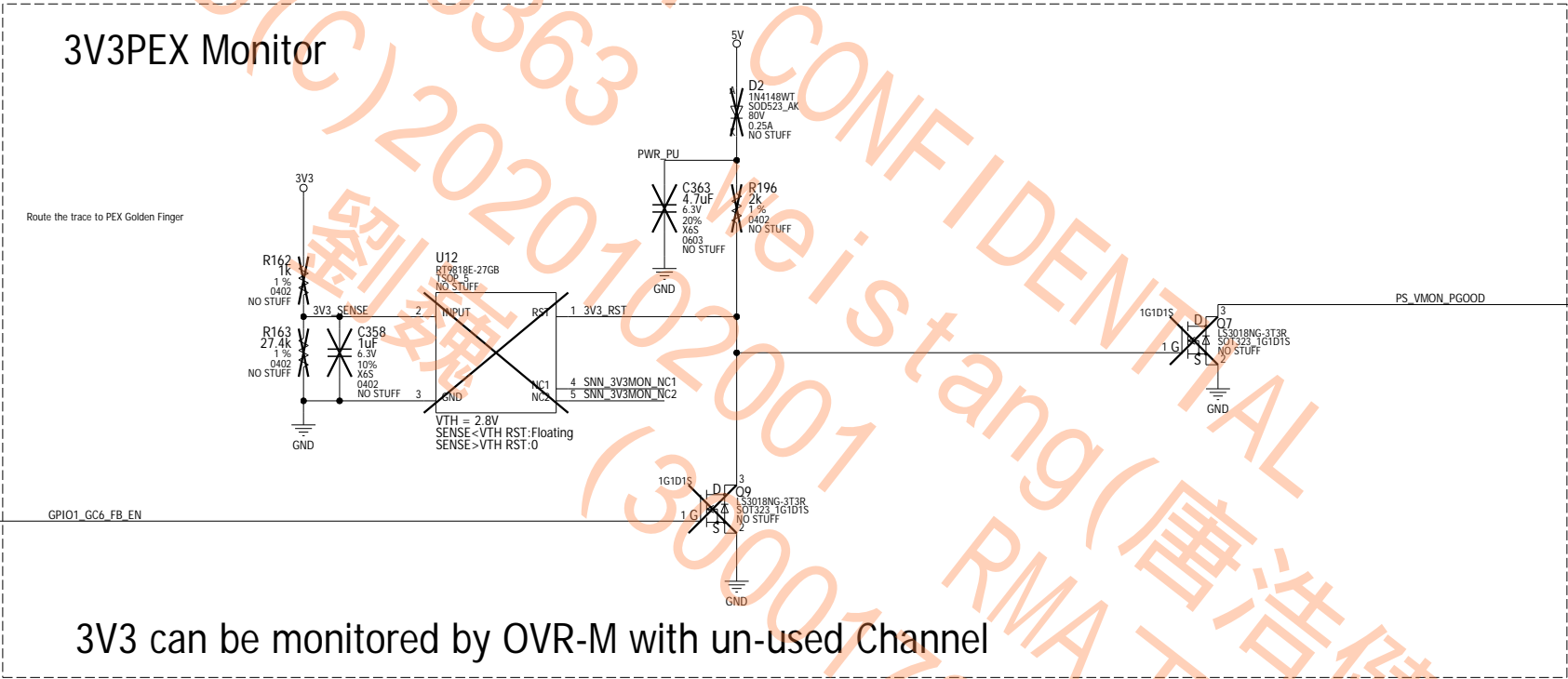


SEQUENCE:NV,PEX,FB ENABLE



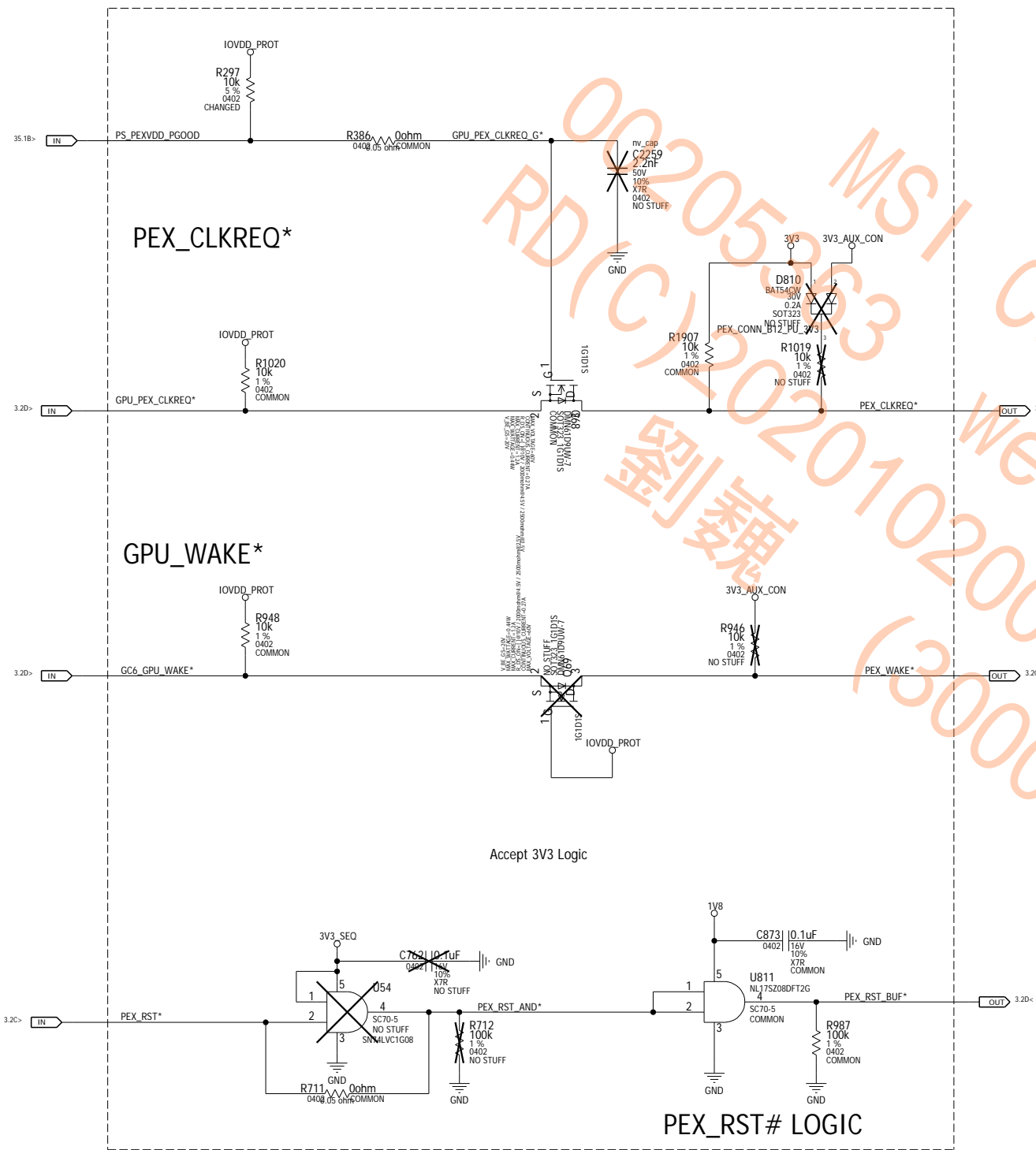
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Sequence: 3V3 MONITOR



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SEQUENCE:MISC

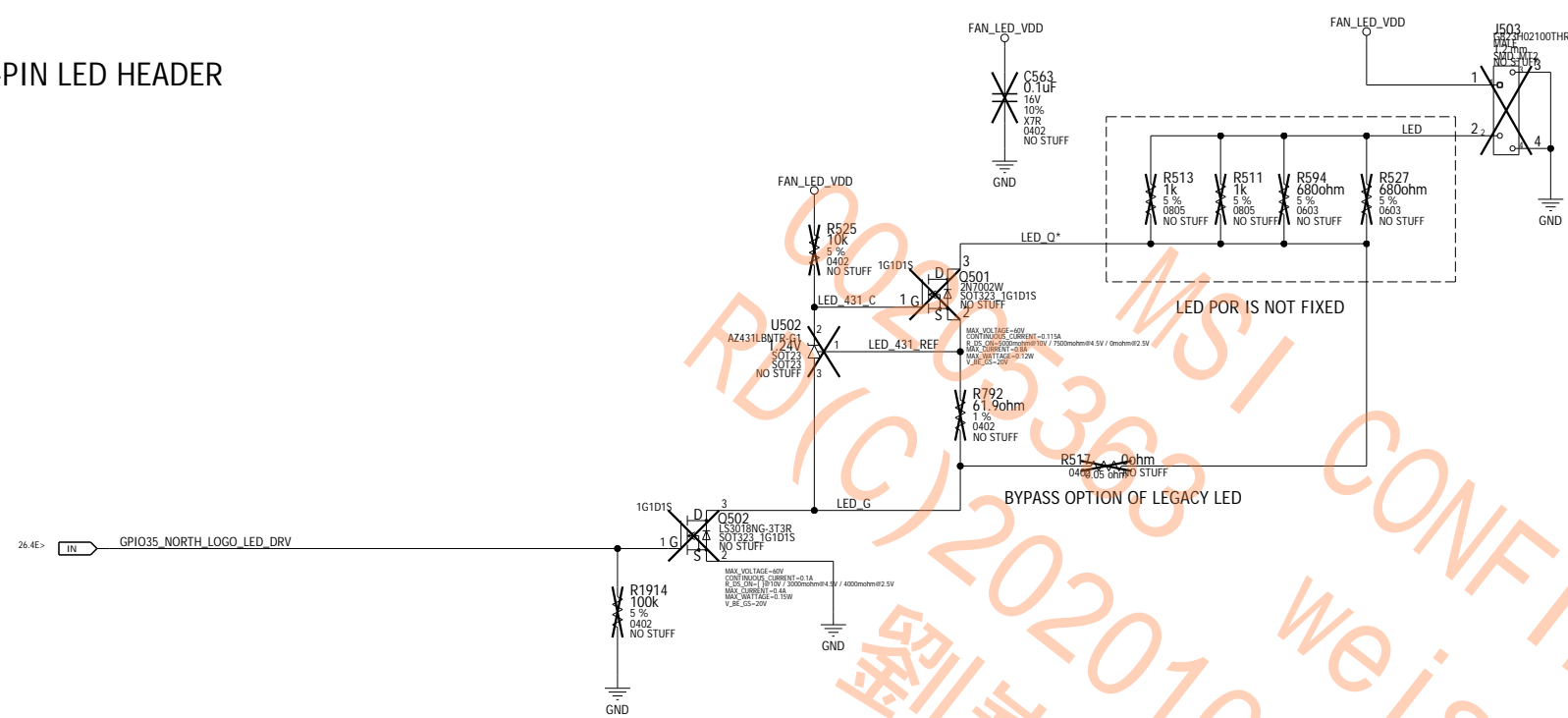


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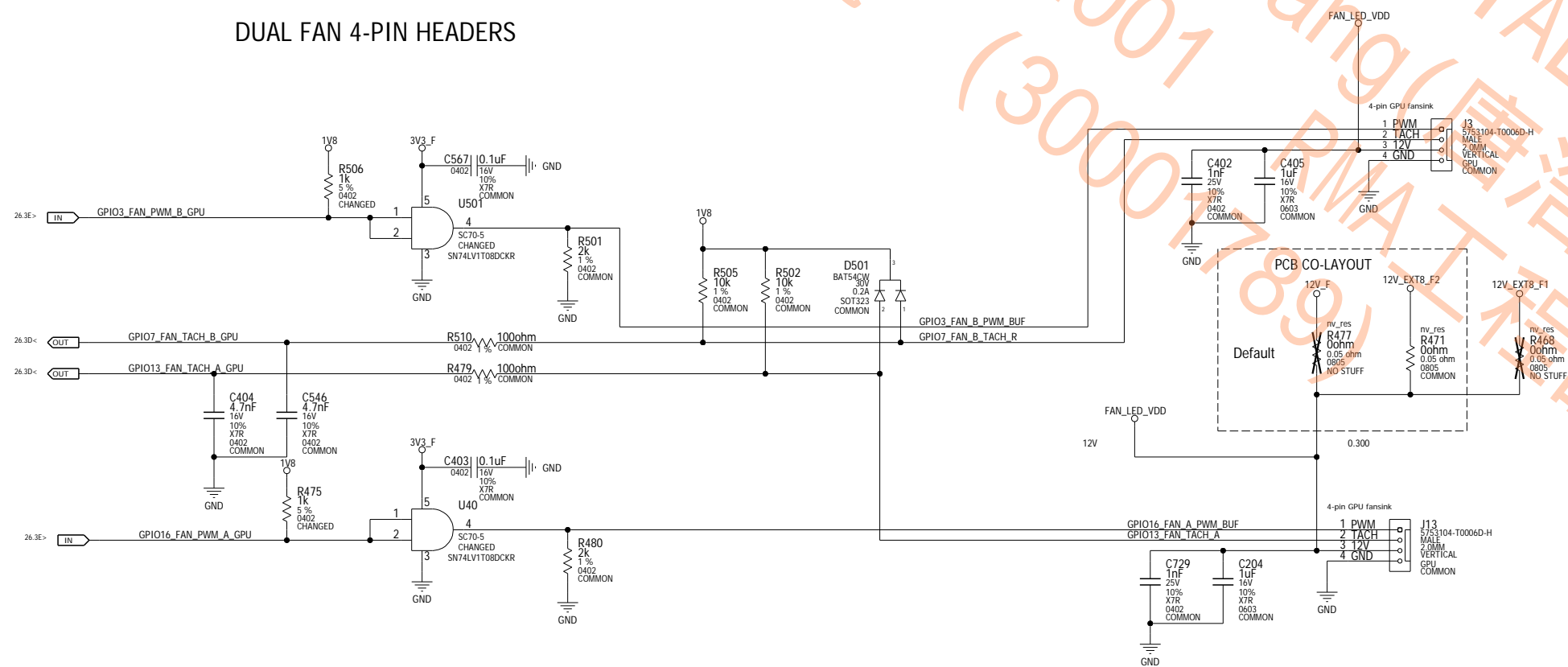
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MISC: LED & FAN

## 2-PIN LED HEADER



## DUAL FAN 4-PIN HEADERS



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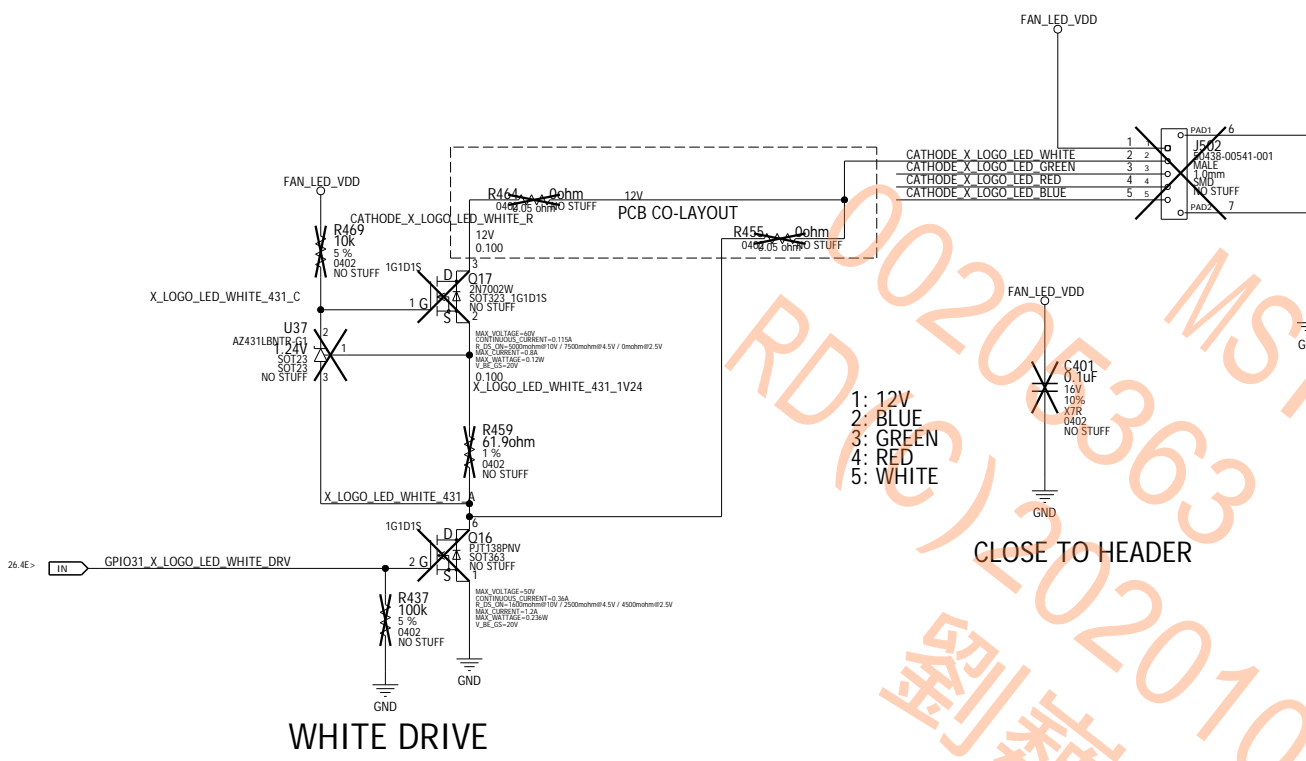
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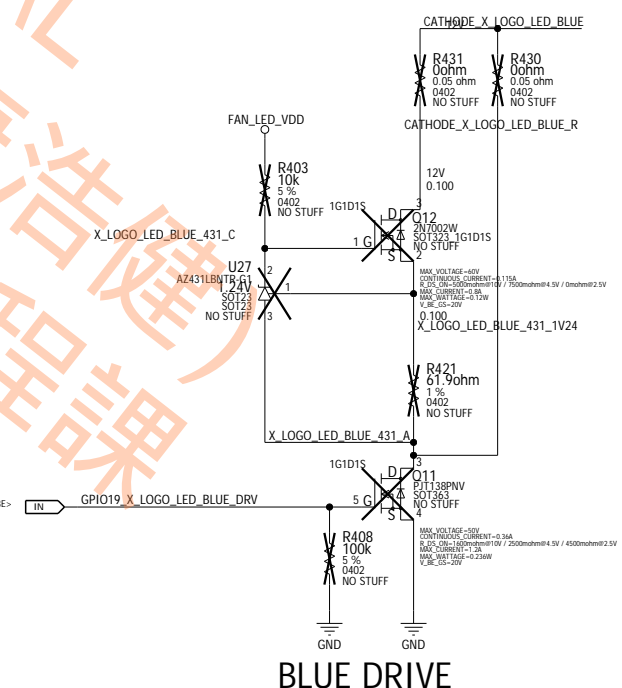
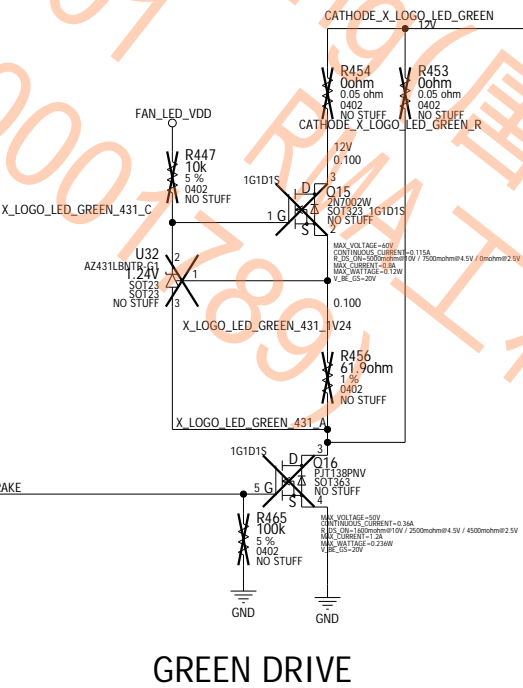
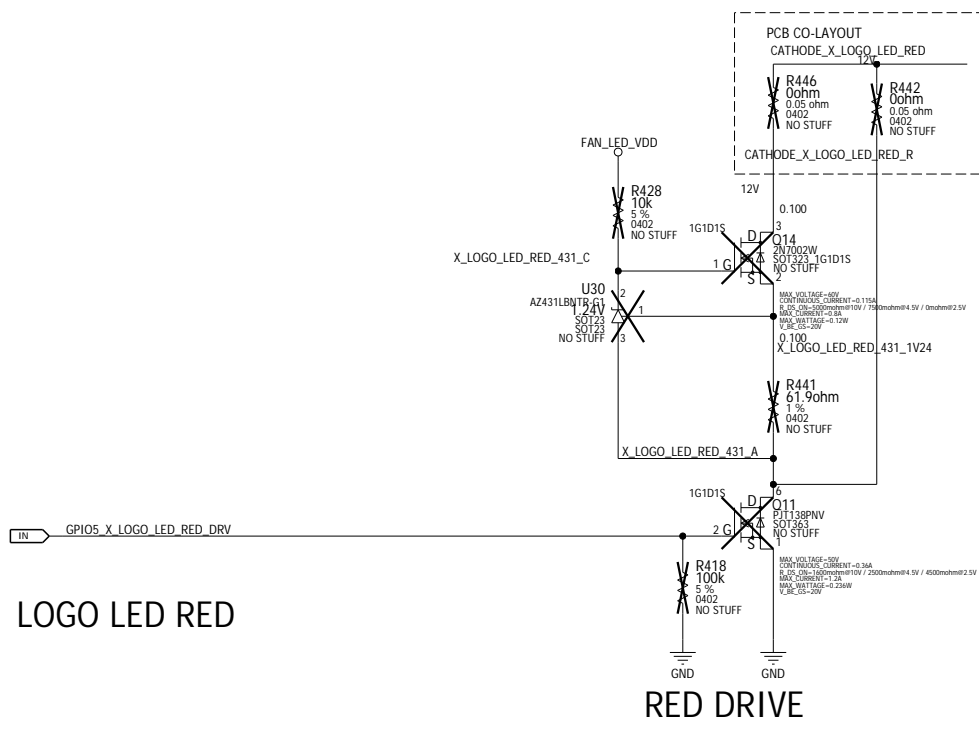
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MISC: RGBW LED REF

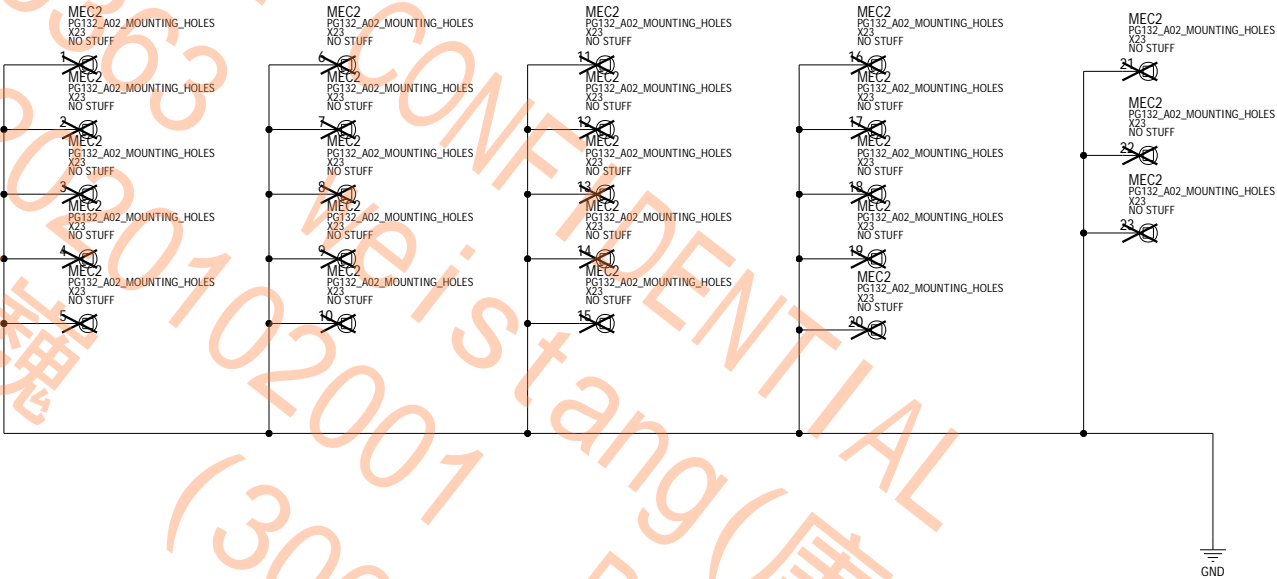
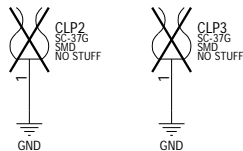


CONNECTOR SIZE TO FIT LAYOUT  
ALL CIRCUIT NO STUFF BY DEFAULT  
ALINGN WITH PASH  
IF ADDITIONAL POWER CONSUPTION R  
NEEDED, IT SHOULD BE ON LED MOD.



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Mechanical: Mounting holes

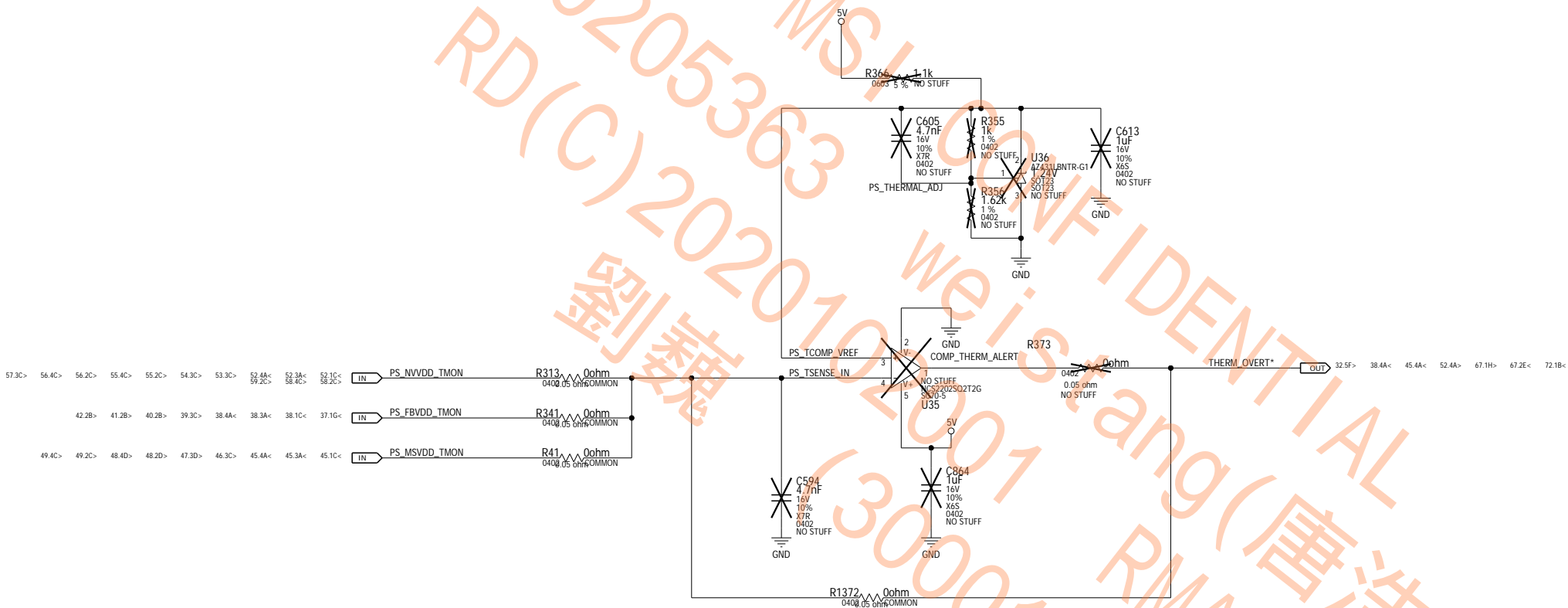


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VR THERMAL PROTECTION



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